Doctoral thesis

Monitoring Function for Gate Oxide Degradation to Improve Reliability of SiC MOSFETs Implemented in Power Conversion Circuits

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Chapter 1

Introduction

1.1 Research Background

1.1.1 Social Background Surrounding Power Electronics

In October 2020, the Japanese government declared its goal of realizing a carbon-neutral, decarbonized society by 2050 [1]. Subsequently, the "Green Growth Strategy" was formulated as an industrial policy to produce a virtuous cycle between the economy and environment [2]. The Green Growth Strategy states that the carbon-neutral goal will be achieved through a society that is "electrified and digitalized in all areas, including manufacturing, services, transportation, and infrastructure." Power electronics systems, which can efficiently convert electric power, are expected to play an important role in the Green Growth Strategy.

In the transportation field, power conversion circuits (so-called VVVF inverters and CVCF inverters in Japan) have already been introduced as propulsion control and auxiliary power supply systems for rolling stock. Fig. 1.1 presents an example of a power conversion circuit for rolling stock. It has been reported that the use of power conversion circuits as propulsion control systems can reduce the

Fig.1.1. Power conversion circuit for rolling stock [3].

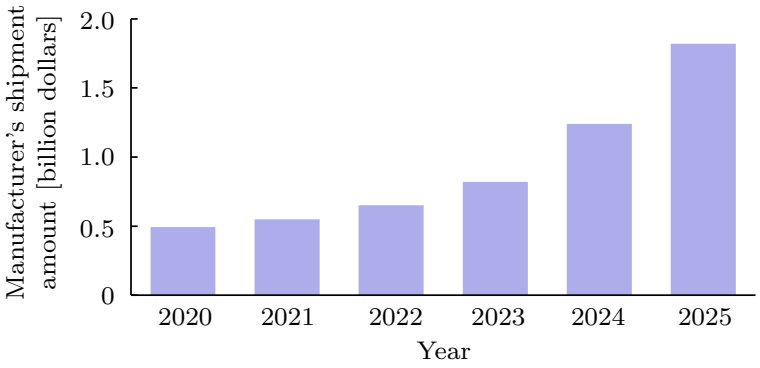


Fig.1.2. Market size forecast for SiC power devices [20].

power consumption of rolling stock by 68% compared to the conventional resistance control systems [4]. These reports suggest that power conversion circuits can be applied to all fields. Of the fields in which the application of power conversion circuits is expected to expand in the future, several require high reliability. As one example, the research and development of power conversion circuits for aircraft has been reported [5]–[9].

1.1.2 Features of SiC Power Devices

In aircraft, the application of power conversion circuits is expected to reduce aircraft weight. 1,700 tons of aviation fuel could be saved per year if each aircraft in operation were 1 kg lighter [6]. For the past 50 years, research and development of power conversion circuits has focused on improving power density and conversion efficiency [10]. It is anticipated to achieve its expectations.

The practical use of power devices based on silicon carbide (SiC), which offers a better performance in power devices compared to Si, is expanding across various applications [11]–[18]. SiC power devices are attracting attention as key devices to further improve the power densities of power conversion circuits. In 2013, the world's first commercialized propulsion control system for rolling stock, using SiC metal-oxide-semiconductor–field-effect transistors (MOSFETs), was released [19]. Fig. 1.2 depicts the market size forecast for SiC power devices [20]. As shown in Fig. 1.2, the market for SiC power devices is expected to expand steadily in the

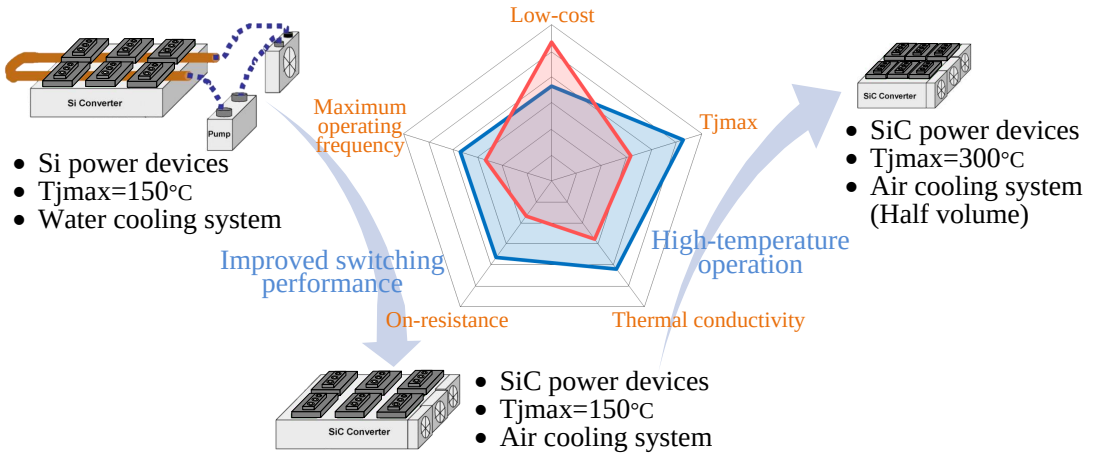


Fig.1.3. High performance of a power conversion circuit exploiting the features of SiC power devices [21].

future.

Power conversion circuits using SiC power devices can be made with improved power densities and lower costs, by exploiting features of SiC power devices. Fig. 1.3 illustrates the high performance of a power conversion circuit that implements features of SiC power devices [21]. Power conversion circuits can be made with improved power densities by improving their switching performance and operating them at high temperatures through the use of SiC power devices. In addition, the cost of power devices alone is less than that of Si, though the power conversion circuits can be shrunk by simplifying the cooling system.

However, SiC power devices have been reported to degrade under long-term use [22]–[25]. For applications that require high reliability, in addition to the power density and conversion efficiency (performance indicators required for power conversion circuits), long-term reliability is also required [26][27].

1.1.3 Failure Factors of Power Conversion Circuits

According to reports investigating the failure factors of power conversion circuits, power devices have the highest failure rate of all components. Fig. 1.4 shows the data summarizing the failure factors of power conversion circuits. As shown, power devices account for one-third of the failure factors in power electronic equip-

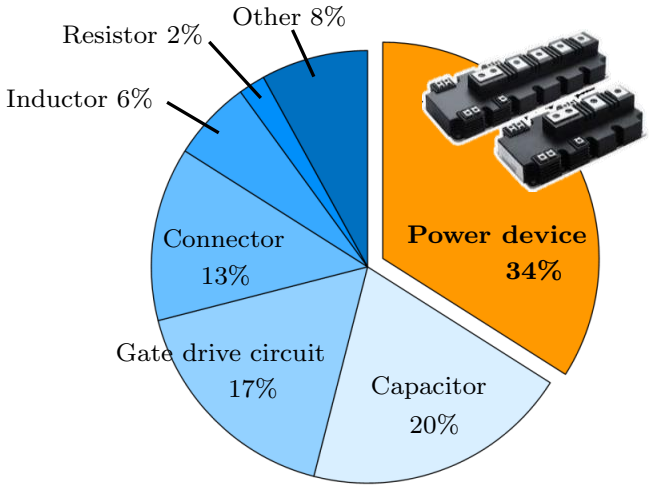
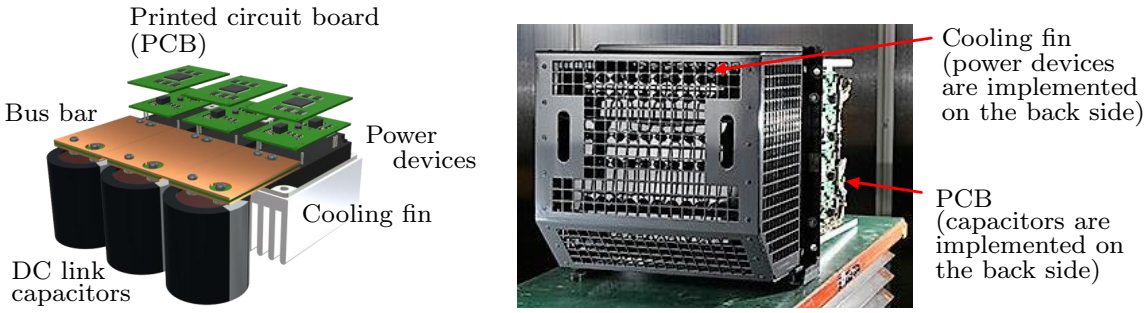


Fig.1.4. Failure factors of power conversion circuits [28].



(a) Schematic diagram (b) Power unit for rolling stock [30]

Fig.1.5. Power unit structure.

ment [28]. Certain reports also indicate that power devices account for half of all failure factors [29]. When power devices fail, "downtime" occurs, and the power conversion circuit cannot be operated. In the case of power conversion circuits for rolling stock, downtime due to power device failures can exceed one year, making extended downtime an issue. Therefore, to improve the long-term reliability of power conversion circuits, an effective strategy is to suppress power device failure.

In many cases, owing to the high power density of power conversion circuits, the components are often unitized or implemented in complex ways. In this dissertation, the unit containing the power device is referred to as the "power unit." Fig. 1.5 shows its structure. In particular, DC link capacitors and bus bars are implemented near to power devices; these turn the current on and off at high

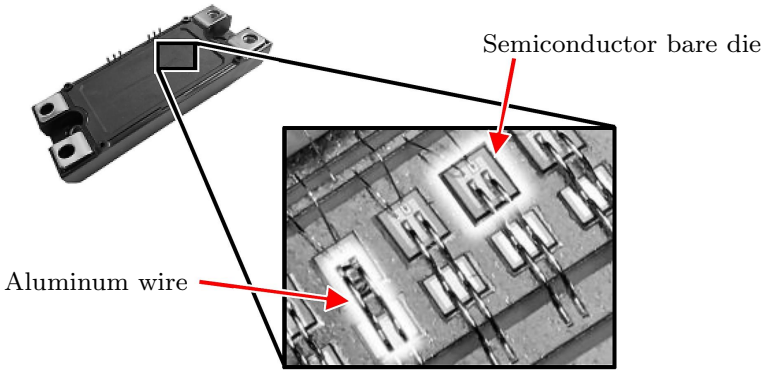


Fig.1.6. Power device and its internal structure.

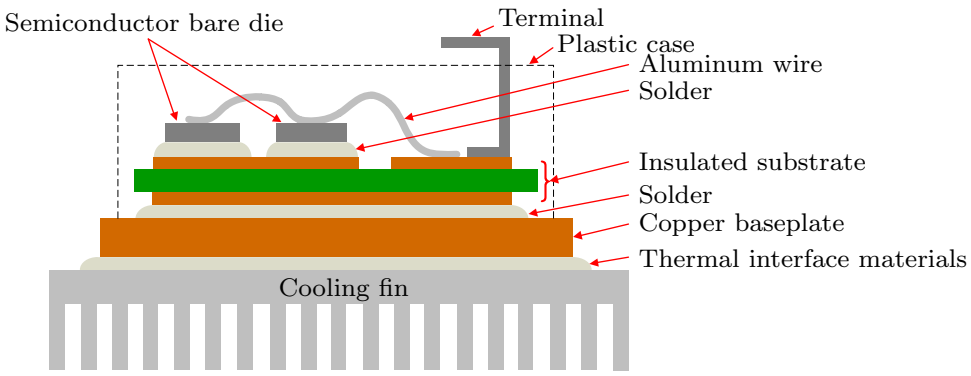
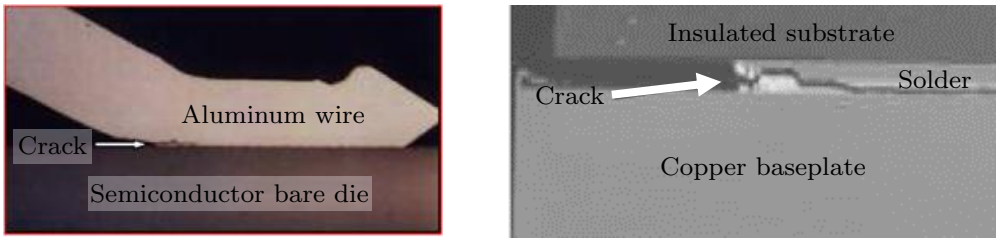


Fig.1.7. Schematic diagram of a power device structure [32].

speeds, to suppress the generation of overvoltage and electromagnetic noise. In addition, power devices are coated uniformly with a thermal interface material to a predetermined thickness and are fastened to the cooling system with a predetermined torque, to maximize cooling performance. Such structures suffer from poor maintainability, and users are unable to disassemble the area around the power devices during maintenance. Therefore, a unified maintenance method for power devices has yet to be established; this is one of the reasons why these devices make up a large percentage of failures [31].

1.1.4 Failure Factors of Power Devices

Power devices consist of a semiconductor bare die enclosed in a package that provides electrical and thermal interfaces. Fig. 1.6 shows a power device and its internal structure. Fig. 1.7 presents a schematic diagram of a power device struc-



(a) Aluminum wire wear-out (b) Solder crack

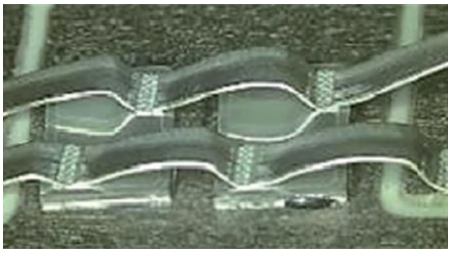
Fig.1.8. Package degradation [32].

ture. Failure factors of power devices can be broadly classified into two categories: "package degradation" and "semiconductor bare die degradation." This dissertation focuses on semiconductor bare die degradation. In this section, both types of degradation are described, and the reason for focusing on semiconductor bare die degradation is clarified.

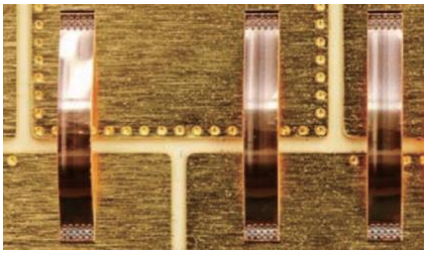
In addition, this dissertation does not cover power device failures caused by temporary stress (e.g., overvoltage or overcurrent). In other words, the focus is upon degradation attributable to long-term use. The reason for this is that power device failures caused by temporary stresses have been investigated for failure prevention by protection circuits. However, protection circuits cannot prevent random failures attributable to individual differences or wear-out failures due to lifetime.

Package degradation includes aluminum wire wear-out and solder cracks. Fig. 1.8 illustrates both types. These degradations occur because of repeated thermal swings in the power and heat cycles, which are themselves caused by the different thermal expansion coefficients of the materials that compose the power module (e.g., aluminum wire, semiconductor bare die, and insulating substrate). Package degradation is the main cause of wear-out failures in Si-insulated gate bipolar transistors (IGBTs), which are currently the most widespread power devices [33][34]. Therefore, new packaging technologies are being developed to improve their long-term reliability [35]–[37].

Fig. 1.9 depicts a technique that uses ribbon bonding instead of aluminum wire.



(a) Aluminum ribbon [38]



(b) Copper ribbon [39]

Fig.1.9. Ribbon bonding.

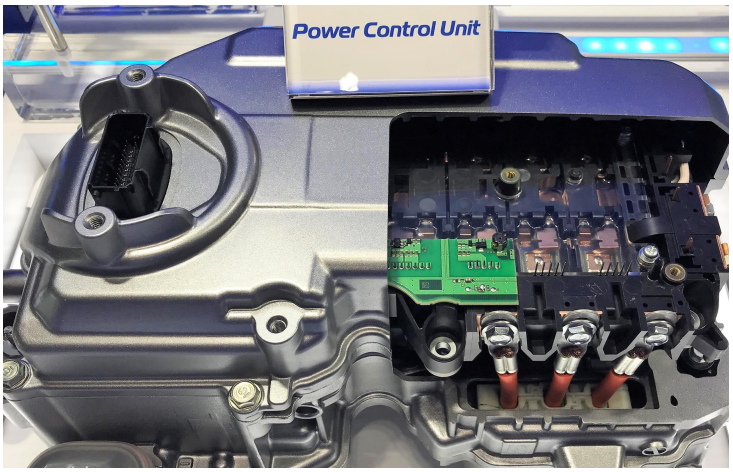


Fig.1.10. Cutaway model of an automotive power conversion circuit.

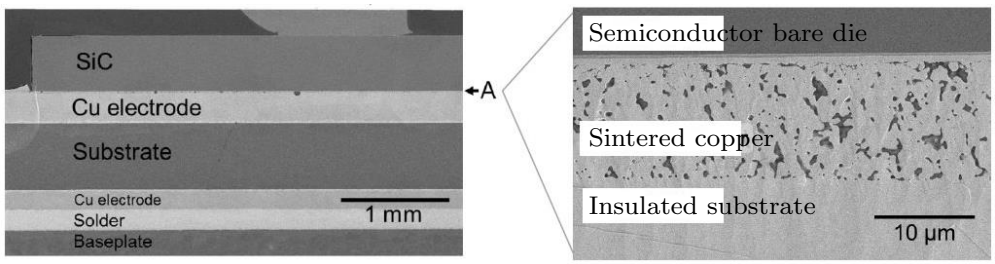


Fig.1.11. Bonding by sintered copper [40].

The two types of ribbon material, aluminum and copper, have both been reported to offer improved long-term reliability compared to aluminum wire [36]. Fig. 1.10 shows a cutaway model of an automotive power conversion circuit. As shown in Fig. 1.10, copper ribbon bonding technology has been put to practical use in several power devices.

Fig. 1.11 shows a technology that uses sintered copper instead of solder as the bonding material [40]. In addition to sintered copper, bonding techniques using

sintered silver have also been reported; both have been shown to improve long-term reliability compared to solder [36].

However, according to research into the long-term reliability of SiC MOSFETs, the issue of semiconductor bare die degradation remains to be improved [23]. In particular, gate oxide has been cited as a degradation factor [41]–[43]. The defect density in the gate oxide of SiC MOSFETs is two orders of magnitude higher than that of Si MOSFETs [44]. As a result, fluctuations of gate threshold voltage and on-resistance attributable to bias temperature instability (BTI) have been reported [22][45][46]. Characteristic power device fluctuations caused by BTI can lead to unreliability in power conversion circuits: If the gate threshold voltage decreases, a short circuit failure of the power device occurs because of the false ON; if the on-resistance increases, the power device cannot be cooled as designed, leading to thermal runaway: furthermore, in power devices implemented in parallel, unbalanced switching transient currents (attributable to mismatch in the gate threshold voltage) and unbalanced steady-state currents (due to mismatch in on-resistance) have been reported [47][48].

In addition, the gate oxide of SiC MOSFETs is subjected to a higher electric field strength than that of Si MOSFETs, owing to the device design [42]. Moreover, the gate oxide of SiC MOSFETs is thinner than that of Si MOSFETs, to ensure a practical gate threshold voltage and low channel resistance. Therefore, the occurrence of gate oxide time-dependent dielectric breakdown (TDDB) is a concern from the perspective of long-term reliability [24], [41], [49]–[54]. Gate oxide TDDB causes short circuit failures in power devices.

Against this background, this dissertation focuses on the semiconductor bare die degradation caused by the long-term use of power devices. In this dissertation, the following definitions are used:

- Degradation: The electrical characteristics of the power device fluctuate with long-term use.

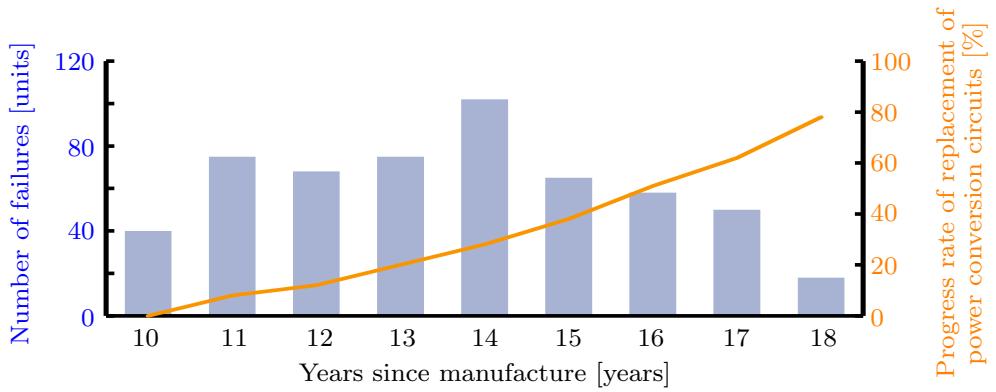


Fig.1.12. Relationship between number of failures and replacement rate of power conversion circuits for a certain type of rolling stock [55].

- Gate oxide degradation: Degradation of power devices due to gate oxide.
- Failure: Malfunctioning of power devices or power conversion circuits.

1.1.5 Maintenance of Equipment

To prevent power-device-failure-induced downtime in power conversion circuits, it is important to detect degradation and undertake maintenance. As described in Section 1.1.3, the components around the power device are unitized; thus, overhauling the power device is not generally undertaken to extend its lifetime. Instead, the entire power unit is replaced with a new one in power-device maintenance.

Fig. 1.12 shows the relationship between the number of failures and the replacement rate of the power conversion circuit for a certain type of rolling stock [55]. Fig. 1.12 shows that the number of failures tends to increase as the number of years since the manufacture of the power conversion circuit increases. On the other hand, the number of failures tends to decrease as the progress rate of replacing the power conversion circuit increases. Therefore, the implementation of appropriately timed maintenance is necessary to improve the long-term reliability of power conversion circuits.

The following section describes existing maintenance methods and considers the appropriate timing for undertaking maintenance on power devices. Fig. 1.13 shows the classification of maintenance methods [56]. Maintenance methods can be

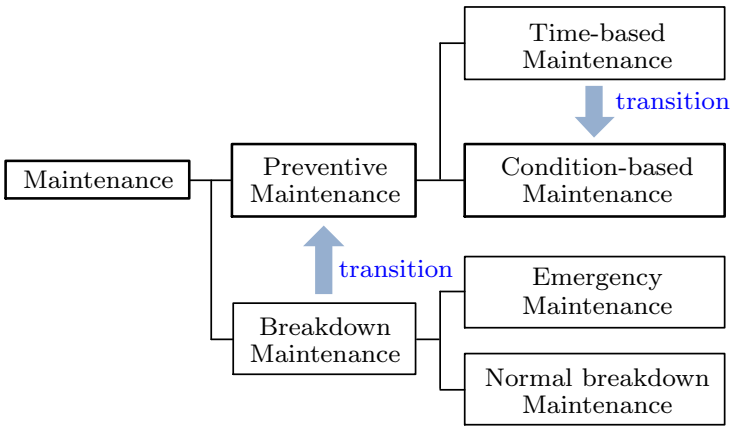


Fig.1.13. Classification of maintenance methods.

broadly classified into two categories: "breakdown maintenance," in which maintenance is performed after failures have occurred, and "preventive maintenance," in which maintenance is performed periodically prior to failures. Breakdown maintenance can often lead to serious equipment failure. Therefore, the downtime tends to be longer, and maintenance costs tend to be higher. Preventive maintenance can be further divided into two types: "time-based maintenance" and "condition-based maintenance." In time-based maintenance, a maintenance period is determined in advance, and maintenance is performed during each period. Time-based maintenance is the mainstream method for the above-mentioned power conversion circuits for rolling stocks. In Japan, the law requires that maintenance be performed on important rolling stock components every four years or every 600,000 km. Furthermore, the power unit is generally replaced with a new one every 10–20 years. However, time-based maintenance can allow failures to occur before the maintenance period is up, owing to differences in the operating environment and equipment.

Against this background, condition-based maintenance has been attracting attention as a new maintenance method. This method monitors the condition of equipment during operation, to detect signs of degradation and perform maintenance before a failure occurs [57]–[78]. The condition of the equipment is moni-

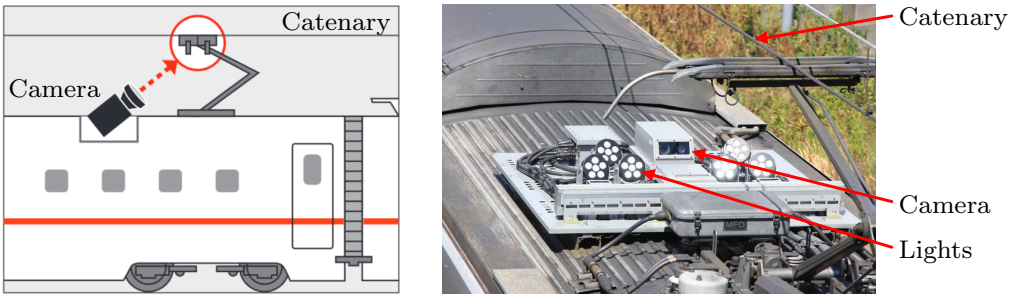


Fig.1.14. Example of a condition monitoring system (catenary monitoring system) [79].

tored by collecting information about the equipment during operation using pre-installed sensors. Condition-based maintenance not only reduces the failure rate and improves long-term reliability: it also contributes to reduced downtime and maintenance costs. Fig. 1.14 shows a catenary monitoring system, one of the condition monitoring systems used in railroad applications. The catenary monitoring system can measure the thickness of the catenary using a camera mounted on the roof of the rolling stock during operation [80]. By referring to the measured data, maintenance can be performed before the catenary breaks, thereby preventing the rolling stock from being suspended due to breakage of the catenary.

On the other hand, a condition-based maintenance method for power conversion circuits has not been established. Condition monitoring technology for power devices also remains in the research phase. If the condition monitoring technology for power devices is established, it will not only reduce the downtime caused by power device failures but also improve the performances and reduce the costs of power conversion circuits, by controlling SiC power device usage.

1.2 Objective and Overview

The objective of this study is to establish a condition monitoring technology for power devices (which are the main cause of failure), to improve the long-term reliability of power conversion circuits. To this end, we present a study related to the condition monitoring of power devices.

First, the target power devices are chosen as SiC MOSFETs, whose applicability is expected to expand in the future. Then, this study focuses on gate oxide degradation, one of the major failure factors of SiC MOSFETs. In addition, because a trade-off relationship pertains between the long-term reliability of the gate oxide and SiC MOSFET performance, it is important to clarify the degradation mechanism of the gate oxide. Establishing a condition monitoring technology for the gate oxide may also be useful for clarifying the degradation mechanism.

Next, to achieve the research objectives, the following three steps were taken.

Step 1

Theoretical study of electrical characteristics suitable for condition monitoring of SiC MOSFETs.

(In this dissertation, the electrical characteristics subject to condition monitoring are referred to as the "aging precursors.")

- Challenge
  - What aging precursor is suitable for condition monitoring?
- Result
  - Theoretical studies suggest that the input capacitance C_{iss} (the voltage-dependent capacitance of MOSFETs) is a suitable aging precursor for condition monitoring.

Step 2

Verification of the validity of Step 1 by actual measurement of the degradation characteristics of SiC MOSFETs.

- Challenge
  - How are degradation characteristics of SiC MOSFETs in a power conversion circuit evaluated?
- Results
  - Development of accelerated aging test circuit under continuous switching conditions.

- Actual measurement of degradation characteristics using the developed accelerated aging test circuit and verification of the validity of Step 1.

Step 3

Development of a measurement circuit for detecting degradation in a power conversion circuit.

- Challenge
  - How is the input capacitance C_{iss} measured in the power conversion circuit?
- Result
  - A gate drive circuit is proposed to measure the input capacitance C_{iss}.

Finally, the condition monitoring technology of the power device is proposed from the research results.

1.3 Dissertation Structure

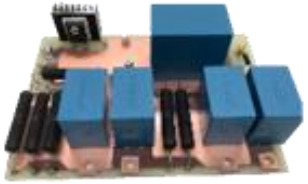
Fig. 1.15 presents the structure of this dissertation. This dissertation proposes a condition monitoring technology for power devices; it is organized into the following chapters.

Step 1: Theoretical study of electrical characteristics suitable for condition monitoring of SiC MOSFETs

Clarification of issues and theoretical study of degradation characteristics through **Chapter 2: Previous Studies and Literature Review**

Step 2: Verification of the validity of Step 1 by actual measurement of the degradation characteristics of SiC MOSFETs

Chapter 3: Accelerated Aging Test Circuit for Power Devices Applying Continuous Switching

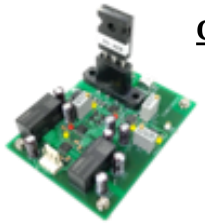


- Development of accelerated aging test circuit

Chapter 4: Characteristic fluctuations of SiC MOSFETs due to oxide charge

- Testing with developed test circuit
- Evaluation of degradation characteristics

Step 3: Development of a measurement circuit for detecting degradation in a power conversion circuit



Chapter 3: Measurement Circuit for Condition Monitoring

- Development of measurement circuit with condition monitoring function
- Operation verification through experiments

The condition monitoring technology of the power device is proposed

Fig.1.15. Dissertation Structure.

Chapter 1

Chapter 1 introduces the social background surrounding power electronics, as well as issues related to the failures of power conversion circuits. Power conversion circuits, which are expected to expand their application range in the future, must have a high power density and high efficiency, as well as long-term reliability. Therefore, it is important to prevent the power-conversion-circuit downtime caused by power device failures. This chapter summarizes the issues in current power device failures and maintenance methods. Moreover, this chapter clarifies the importance of establishing condition monitoring technology for power devices. Then, the objectives of the study are described.

Chapter 2

Chapter 2 summarizes the previous literature regarding condition monitoring techniques for power devices. The benefits and drawbacks of aging precursors that have already been proposed for power-device condition monitoring are summarized. As a result, the current situation (in which a unified aging precursor has not been decided) is clarified. In addition, a literature survey is performed to investigate the fluctuation characteristics of power devices caused by gate oxide degradation. Through literature reviews, it is theoretically shown that the input capacitance C_{iss} (which is the voltage-dependent capacitance), is suitable for aging precursors.

Chapter 3

Chapter 3 describes the development of the accelerated aging test method for power devices. The purpose of the accelerated aging test in this study is to clarify the degradation characteristics of power devices implemented in power conversion circuits. Therefore, the test circuits that can undergo accelerated aging under the continuous switching condition, as well as the actual use conditions of power devices, are developed. In the development

of the test circuits, a design method that does not spread failures to the test circuits is proposed, considering the failure of the device during the test.

Chapter 4

In Chapter 4, two types of accelerated aging tests for power devices are performed using the test circuit developed in Chapter 3, to verify the theoretical considerations in Chapter 2 using actual measurements. In the first type, multiple test conditions are applied to a single type of device under testing. In the second type, a single test condition is applied to multiple types of device under testing. The results of the two experimental verifications demonstrate the effectiveness of the proposed accelerated aging test method. In addition, the input capacitance C_{iss} with respect to the gate–source voltage v_{GS} characteristic (C_{iss}–v_{GS} characteristic), which is proposed as an aging precursor for condition monitoring in this dissertation, is shown to fluctuate with the degradation of power devices. Furthermore, it is shown that the C_{iss}–v_{GS} characteristic fluctuation with respect to temperature is smaller than that under degradation.

Chapter 5

Chapter 5 describes the development of a circuit that can measure the C_{iss}–v_{GS} characteristics in power conversion circuits. It reviews the commonly used methods for measuring the C_{iss}–v_{GS} characteristics, and it discusses methods that can be implemented in power conversion circuits. Then, a gate driver circuit that can measure the C_{iss}–v_{GS} characteristics is proposed. The design method and operation sequence of the proposed gate driver circuit are described. In addition, experiments are performed to show that the proposed gate driver circuit can measure the C_{iss}–v_{GS} characteristics of power devices before and after degradation.

Chapter 6

Chapter 6 describes the conclusions derived from the results obtained in each

chapter, the contribution of this dissertation to the field of power electronics and devices, and the study's prospects.

Chapter 2

Previous Studies and Literature Review

In this chapter, previous studies related to the condition monitoring of power devices are introduced. Through a review of these studies, remaining issues are identified and the issues to be solved in this study are clarified. In addition, the electrical characteristics suitable for the condition monitoring of power devices are theoretically investigated in the literature.

2.1 Studies on Condition Monitoring of Power Devices

To detect signs of degradation in power devices, it is necessary to identify aging precursors suitable for condition monitoring [81][82]. In this section, previous studies regarding the condition monitoring of power devices are reviewed. The main aging precursors proposed in previous studies are summarized in terms of their benefits and drawbacks. Then, the features of the aging precursors suitable for the condition monitoring technology aimed at in this study are discussed.

Fig. 2.1 shows the switching waveforms of MOSFETs and the aging precursors described in this section. As shown in Fig. 2.1, previous studies into condition monitoring techniques [using on-voltage, gate threshold voltage, switching waveforms (turn on switching time, Miller platform voltage) and gate leakage current as aging precursors] are described below.

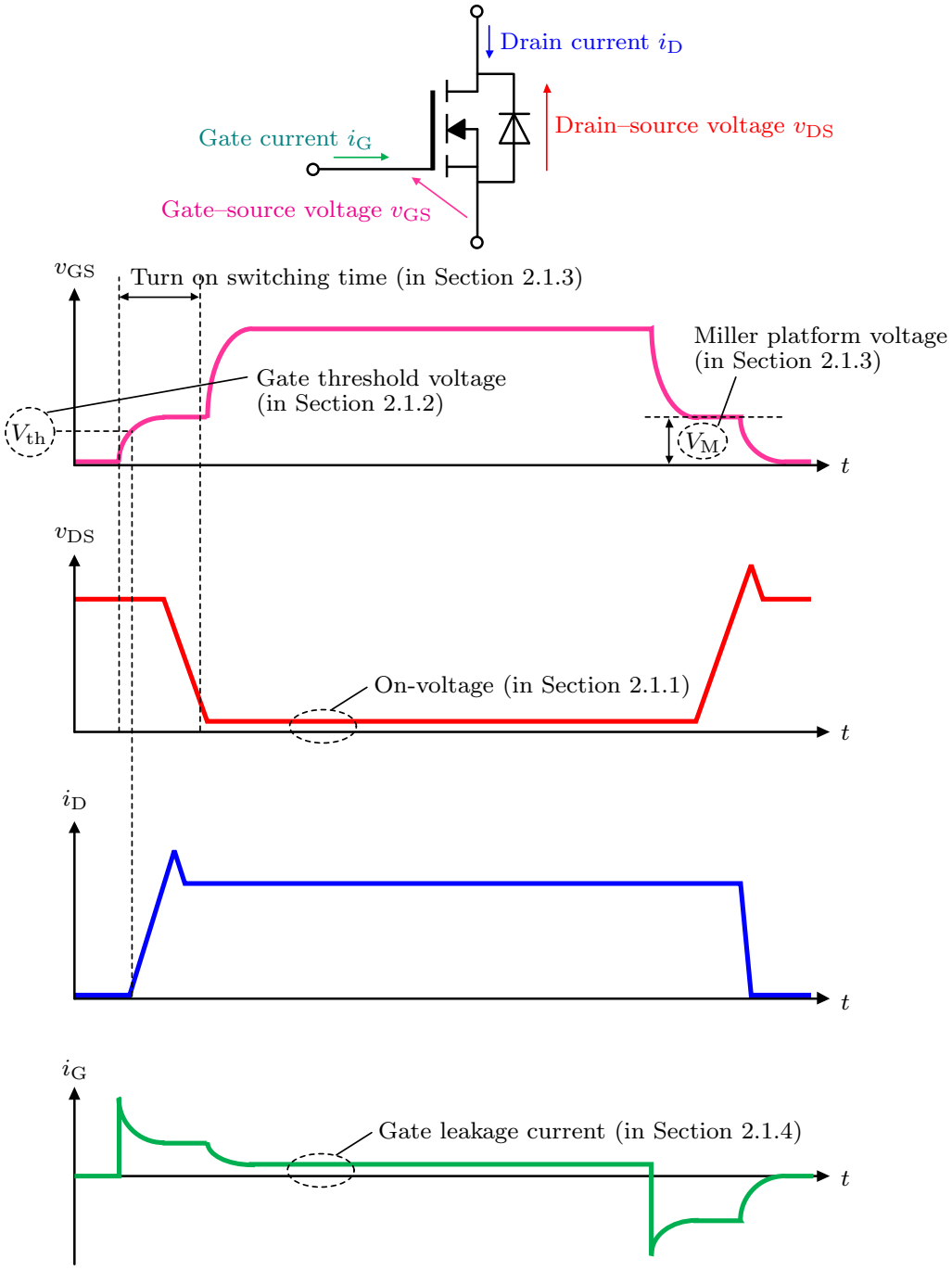


Fig.2.1. Switching waveforms of MOSFETs and the aging precursors described in this section.

2.1.1 On-voltage

On-voltage has been proposed as an aging precursor that can detect the degradation of both the package and semiconductor bare die [34], [83]–[88]. Fig. 2.2 shows the results of the power cycling test as the accelerated aging test for SiC

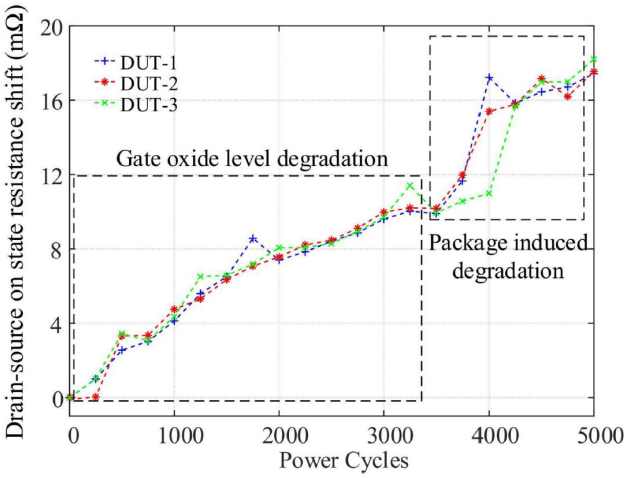
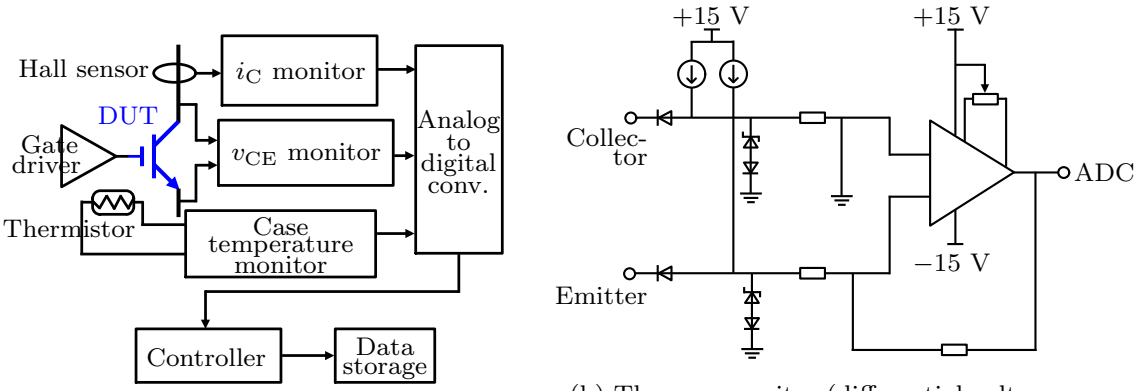


Fig.2.2. Fluctuation of on-resistance in accelerated aging test [86].



(a) Schematic diagram of the system.

(b) The v_{CE} monitor (differential voltage sense circuit).

Fig.2.3. On-voltage measurement system proposed in Ref. [84].

MOSFETs. From Fig. 2.2, both the degradation produced by the gate oxide and the package (bonding wire wear-out) increase the on-resistance (on-voltage).

Fig. 2.3 shows the on-voltage measurement system proposed in Refs. [83][84]. The on-voltage measurement system consists of a current sensor, differential voltage measurement circuit, and thermistor. Fig. 2.4 (i) shows the results of the on-voltage measurement for an IGBT module implemented in a power conversion circuit using the system shown in Fig. 2.3. From Fig. 2.4, it can be seen that the i_C–v_{CE} characteristics of the IGBT module can be measured. However, variation is observed in the measurement data, which may be produced by the electromagnetic noise from the main circuit. In addition, the on-voltage is temperature dependent.

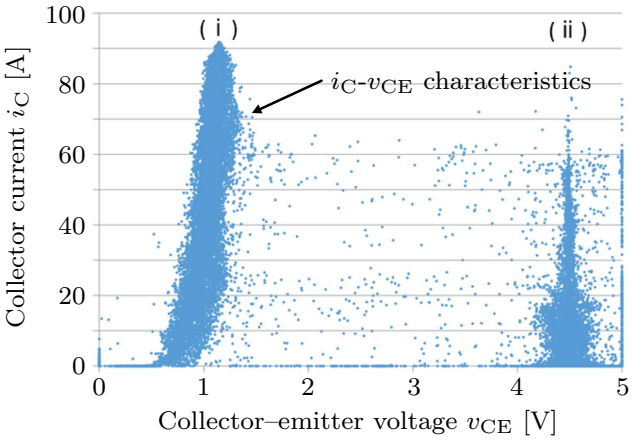


Fig.2.4. Measurement results of the on-voltage in Ref. [86].

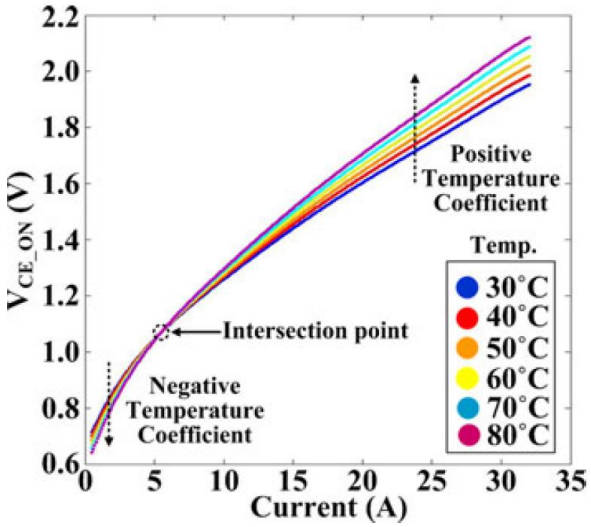


Fig.2.5. i_C–v_{CE} characteristics of an IGBT, with intersection point [88].

Although the case temperature of the IGBT is measured by the thermistor, it is difficult to separate the characteristic fluctuations attributable to degradation and temperature because the case and junction have different heat capacities.

To eliminate the effect of on-voltage fluctuations caused by temperature, Ref. [34] has proposed a method to estimate the power device losses. However, it is difficult to accurately estimate these losses in power conversion circuits during operation.

In addition, it has been proposed in Ref. [88] that the temperature dependence can be eliminated by measuring the on-voltage at the IGBT intersection point. Fig. 2.5 shows the i_C–v_{CE} characteristics of an IGBT, which feature an intersection

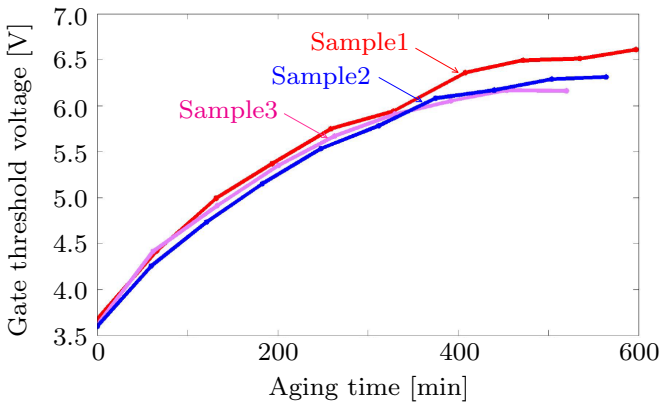


Fig.2.6. Gate threshold voltage fluctuation with respect to HTGB test time for Si MOSFETs [89].

point that is independent of temperature. On the other hand, such intersection points do not exist in SiC MOSFETs; therefore, they cannot be applied to SiC MOSFETs.

2.1.2 Gate Threshold Voltage

Gate threshold voltage has been proposed as an aging precursor that can detect gate oxide degradation [89]. Fig. 2.6 shows the results of the high temperature gate bias (HTGB) test for Si MOSFETs. From Fig. 2.6, the gate threshold voltage can be seen to increase with HTGB test time. However, no measurement circuit has been proposed for condition monitoring. Ref. [90] has proposed a method to measure the gate threshold voltage online during accelerated aging tests; however, the implementation of a similar method in power conversion circuits has not been discussed. Furthermore, the gate threshold voltage is temperature dependent. Therefore, it is difficult to separate the characteristic fluctuations attributable to degradation and temperature. In addition, and similar to the on-voltage precursor, the measurement may be affected by electromagnetic noise from the main circuit.

2.1.3 Switching Waveforms

Switching waveforms have been proposed as aging precursors that can detect the degradation of both the package and semiconductor bare die [29][91]–[94]. Fig. 2.7

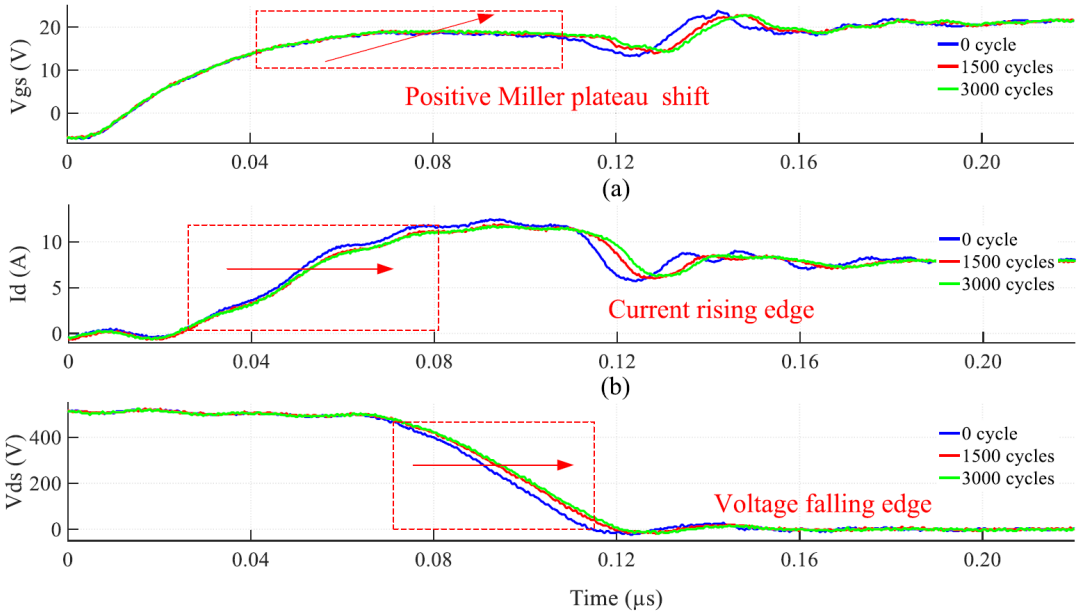


Fig.2.7. Fluctuations of switching waveform in accelerated aging test [29].

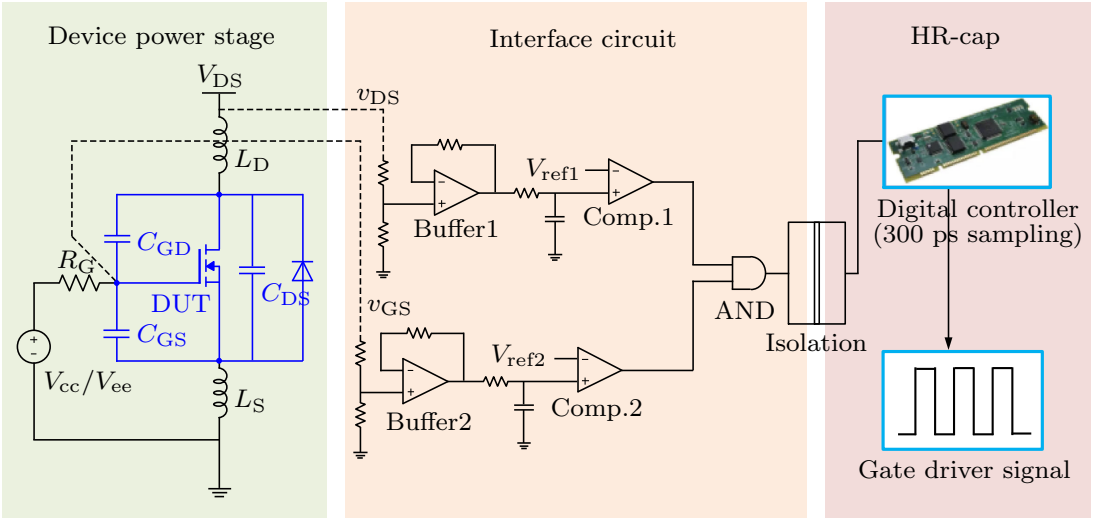
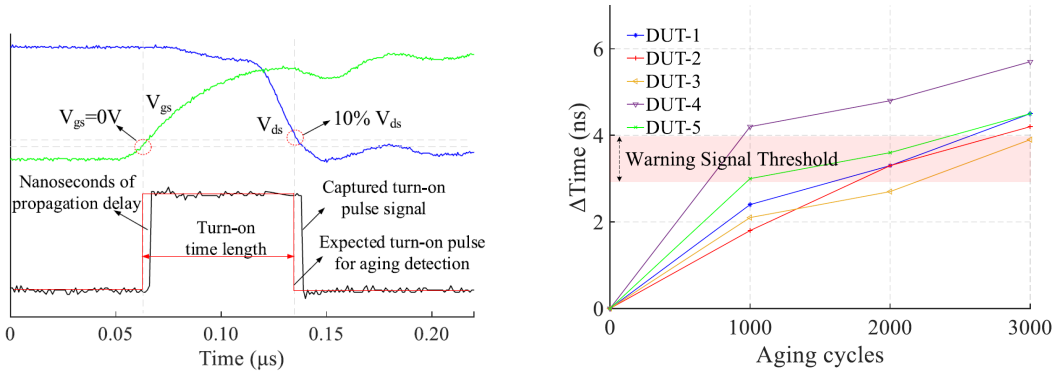


Fig.2.8. Measurement circuit used to measure the switching time [29].

shows the fluctuation of the switching waveform caused by the degradation of SiC MOSFETs [29]. In Fig. 2.7, the power cycling test was performed as an accelerated aging test, and the switching waveforms fluctuated because of the degradation of SiC MOSFETs.

In Ref. [29], the switching time was identified as an aging precursor, based on the fluctuation of the switching waveforms. Fig. 2.8 shows the measurement circuit used for measuring the switching time. This circuit calculates the switching period



(a) Experimental waveforms.

(b) Measurement results for switching time due to degradation.

Fig.2.9. Condition monitoring result of switching time [29].

by measuring the drain–source voltage and gate–source voltage of the MOSFET. Fig. 2.9(a) shows the experimental waveform of the switching time, as measured by the measurement circuit. Fig. 2.9(b) shows the results of the switching time measured by the measurement circuit, which fluctuates due to degradation. In Ref. [91], the Miller platform voltage was identified as an aging precursor, based on the fluctuation of the switching waveforms.

However, a high time resolution is required to measure the switching waveforms. In Ref. [29], a controller with a sampling period of 300 ps was used to detect the fluctuation of the switching time. In addition, the switching waveforms are temperature dependent, and the switching waveforms also depend on the load current. Therefore, it is difficult to separate degradation from characteristic fluctuations attributable to temperature and main circuit operating conditions.

2.1.4 Gate Leakage Current

Gate leakage current has been proposed as an aging precursor to detect gate oxide degradation [95][96]. Fig. 2.10 shows the fluctuation of the gate leakage current caused by the degradation of SiC MOSFETs [95]. In Fig. 2.10, the power cycling test was performed as an accelerated aging test, and the gate leakage current fluctuated owing to the degradation of SiC MOSFETs. Fig. 2.11 shows the

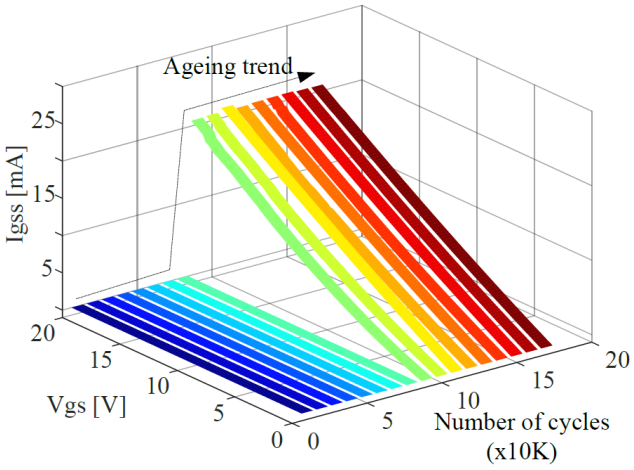


Fig.2.10. Fluctuations of gate leakage current in accelerated aging test [95].

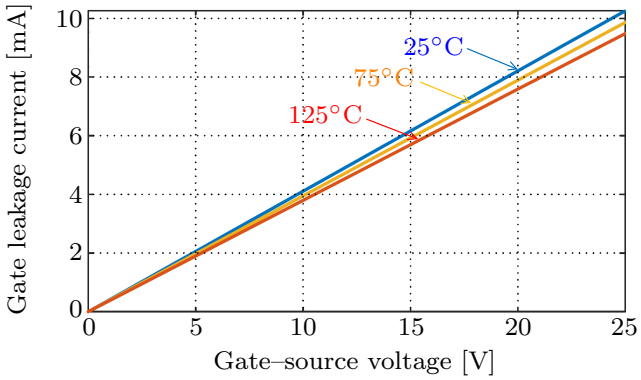


Fig.2.11. Temperature dependence of gate leakage current [95].

temperature dependence of the gate leakage current. Because the temperature dependence is small compared to the degradation-induced characteristic fluctuation, the characteristic fluctuation by temperature can be neglected.

Fig. 2.12 depicts a measurement circuit that can measure the gate leakage current; it was proposed in Ref [95]. The circuit measures the voltage across the gate resistor R_{on}, to thereby measure the gate leakage current. When the gate leakage current exceeds a predetermined threshold, the comparator outputs a signal indicating that the SiC MOSFET has degraded. Fig. 2.13 shows the experimental results when detecting the degradation of SiC MOSFETs using the proposed measurement circuit. In the healthy device under test (DUT), no signal is outputted from the measurement circuit; meanwhile, in the aged DUT, the signal indicating degradation is outputted from the measurement circuit.

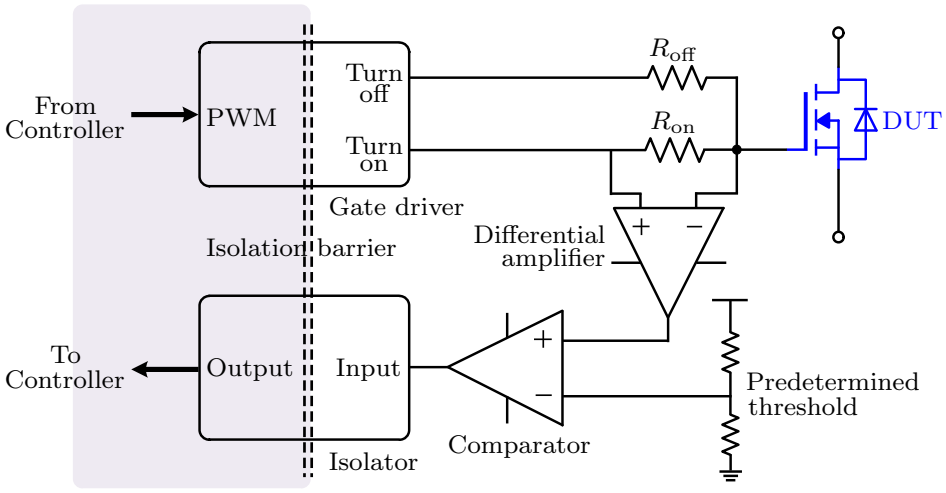


Fig.2.12. Measurement circuit used to measure the gate leakage current [95].

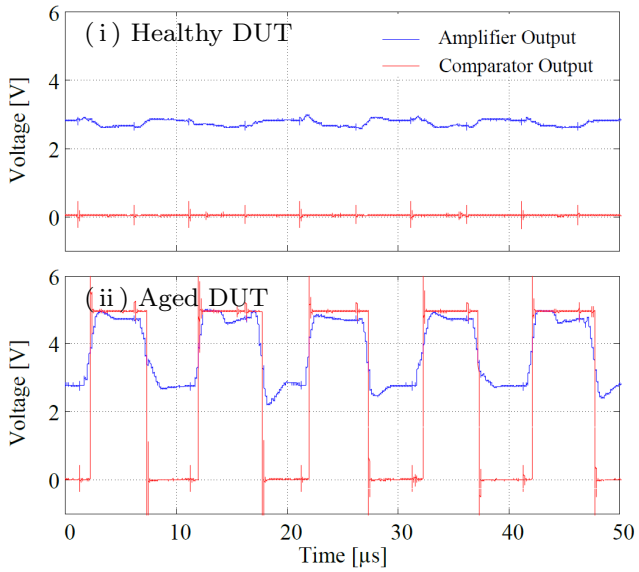


Fig.2.13. Measurement results of gate leakage current switching attributable to degradation [95].

However, the gate leakage current does not consistently change as the gate oxide degradation progresses, and a dramatic increase occurs just before failure. In addition, the only case in which the gate leakage current increases to a detectable value occurs at the soft breakdown. At the hard breakdown, the time between the increase to a detectable value and the failure is short. Therefore, it is not suitable as an aging precursor for early warning, and it is not suitable for condition monitoring.

Table.2.1 Features of aging precursors of power devices for condition monitoring.

Sec.	Aging precursors	Temperature dependence	Other comments
2.1.1	On-voltage	✓	Dependency on operating conditions
2.1.2	Gate threshold voltage	✓	–
2.1.3	Switching waveforms	✓	Dependency on operating conditions
2.1.4	Gate leakage current	–	Not always fluctuating due to degradation

2.1.5 Summary of Features of Aging Precursors

Tab. 2.1 summarizes the features of the aging precursors introduced in Sections 2.1.1–2.1.4. As shown in Tab. 2.1, electrical characteristics that fluctuate with respect to gate oxide degradation and have a small temperature dependence are suitable as aging precursors for condition monitoring. It is necessary to identify new aging precursors offering such characteristics.

2.2 Theoretical Consideration of Gate Oxide Degradation

In this section, the aging precursors considered suitable for the condition monitoring considered in this study are theoretically considered and identified through a literature review.

2.2.1 Changes in Oxide Charge and Characteristic Fluctuations of Power Devices

Prior to the identification of aging precursors, the occurrence of gate oxide degradation in MOSFETs is investigated theoretically.

Fig. 2.14 shows the oxide charge Q_{ox} in the gate oxides grown on semiconductor surfaces [97]. In the gate oxides of MOSFETs, the oxide charge Q_{ox} change is attributable to the change with respect to the degradation process of the mobile charge Q_{M}, fixed charge Q_{F}, and trapped charge Q_{T} in the gate oxide. Neglecting the effect of the interface charge Q_{I} at the gate oxide-semiconductor interface, the

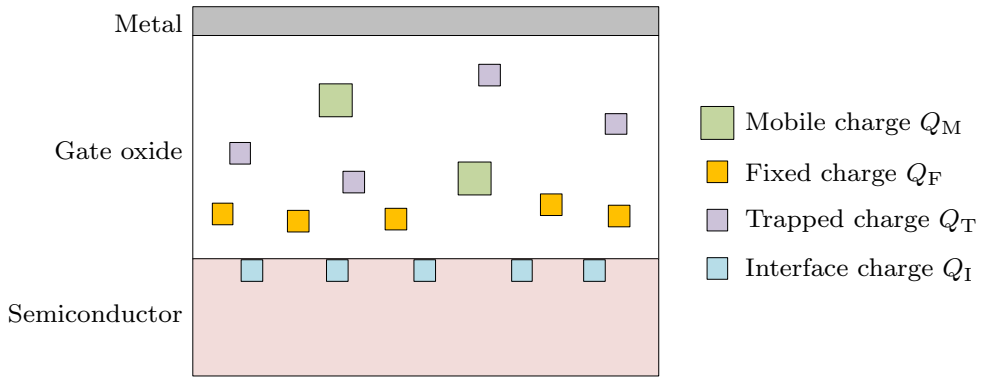


Fig.2.14. Gate oxide charge Q_{ox} in the gate oxide grown on semiconductor surfaces [97].

oxide charge Q_{ox} can be given by the following equation [98]:

$$Q_{ox} = Q_M + Q_F + Q_T. \tag{2.1}$$

The change of the oxide charge Q_{ox} produces various fluctuations in the electrical characteristics of the MOSFET. For example, the gate threshold voltage V_{th} is given by [97]

$$V_{th} = \frac{\sqrt{4\varepsilon_s kTN_A \ln(N_A/n_i)}}{C_{ox}} + \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) - \frac{Q_{ox}}{C_{ox}}, \tag{2.2}$$

where ε_s is the dielectric constant for the semiconductor, k is Boltzmann's constant, T is the absolute temperature, N_A is the acceptor density in the P-base region, n_i is the intrinsic carrier concentration, C_{ox} is the specific capacitance of the gate oxide, and q is a quantum of electricity. From Eq. 2.2, it can be seen that the gate threshold voltage V_{th} fluctuates under the change of the oxide charge Q_{ox}.

The channel resistance R_{CH}, which forms the on-resistance $R_{DS(ON)}$ of the MOSFET, is given in the linear region by [97]

$$R_{CH} = \frac{L_{CH}}{Z\mu_{ni}C_{ox}(v_{GS} - V_{th})}, \tag{2.3}$$

where L_{CH} is the channel length, Z is the channel width, and μ_{ni} is the inversion layer mobility for electrons. From Eq. 2.3, the channel resistance R_{CH} can be seen to also fluctuate under the fluctuation of the gate threshold voltage V_{th}. On the other hand, Eq. 2.2 includes the absolute temperature T, which indicates

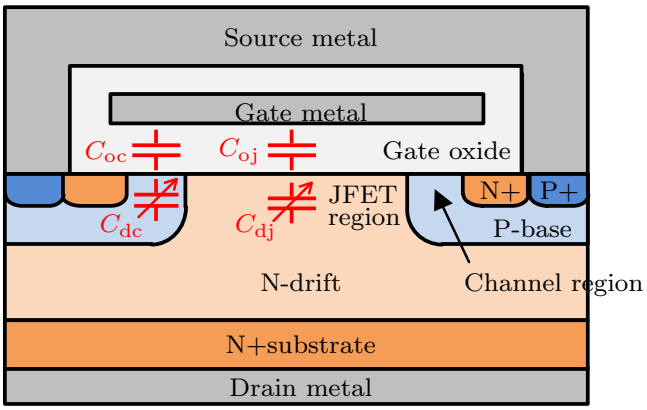


Fig.2.15. Parasitic capacitors around gate oxide.

that the gate threshold voltage V_{th} fluctuates not only because of the change in oxide charge Q_{ox} but also the change in temperature. Even in the channel resistance R_{CH}, the inversion layer mobility for electrons μ_{ni} included in Eq. 2.3 is temperature dependent. In addition, the drift region resistance, which accounts for a large percentage of the MOSFET on-resistance $R_{\mathrm{DS(ON)}}$ along with the channel resistance R_{CH}, also exhibits a temperature dependence. Therefore, the gate threshold voltage V_{th} and the on-resistance $R_{\mathrm{DS(ON)}}$ fluctuate because of the gate oxide degradation and temperature change. Therefore, the gate threshold voltage V_{th} and on-resistance $R_{\mathrm{DS(ON)}}$ are unsuitable aging precursors for condition monitoring.

2.2.2 Theoretical Investigation of Aging Precursor Suitable for Condition Monitoring

In this section, an electrical characteristic that fluctuates with respect to the oxide charge Q_{ox} and is suitable as an aging precursor for condition monitoring is identified.

The depletion layer capacitance of MOSFETs is another electrical characteristic that fluctuates as the oxide charge Q_{ox} changes. Fig. 2.15 shows the parasitic capacitors around the gate oxide: C_{oc}, formed by the gate capacitance between the

gate metal and the P-base region; C_{oj}, formed by the gate capacitance between the gate metal and the JFET region; C_{dc}, formed by the depletion capacitance of the P-base region; and C_{dj}, formed by the depletion capacitance of the JFET region. When the channel region is in the depletion state, the depletion layer capacitance C_{dc} is given by the following equation (for the depletion layer capacitance of a P-type MOS capacitor) [97]:

$$C_{\mathrm{dc}} = \frac{C_{\mathrm{ox}}}{\sqrt{1 + \frac{2C_{\mathrm{ox}}^2(v_{\mathrm{GS}} + Q_{\mathrm{ox}}/C_{\mathrm{ox}})}{qN_{\mathrm{A}}\varepsilon_{\mathrm{s}}}} - 1}. \tag{2.4}$$

Furthermore, when the JFET region is in the depletion state, the depletion layer capacitance C_{dj} is given (when the drain–source voltage $v_{\mathrm{DS}} = 0$ V and assuming the depletion layer capacitance of a N-type MOS capacitor) by [97]

$$C_{\mathrm{dj}} = \frac{C_{\mathrm{ox}}}{\sqrt{1 + \frac{2C_{\mathrm{ox}}^2(v_{\mathrm{GS}} + Q_{\mathrm{ox}}/C_{\mathrm{ox}})}{qN_{\mathrm{D}}\varepsilon_{\mathrm{s}}}} - 1}, \tag{2.5}$$

where N_{D} is the donor density of the drift layer. Equations 2.4 and 2.5 consider the case of an ideal MOS capacitor where there is no work function difference between the metal and semiconductor, and all doped impurities are ionized.

From Eqs. 2.4 and 2.5, it can be seen that the depletion layer capacitances C_{dc} and C_{dj} are voltage-dependent capacitances that depend on the gate–source voltage v_{GS}. In addition, Eqs. 2.4 and 2.5 show that when the oxide charge Q_{ox} changes under gate oxide degradation, the depletion layer capacitance C_{dc} and C_{dj} are affected not only by the applied gate–source voltage v_{GS} but also the oxide charge Q_{ox}. However, Eqs. 2.4 and 2.5 do not include the absolute temperature T, indicating a lack of temperature dependence [*1]. From the aforementioned analysis, the depletion layer capacitance C_{dc} and C_{dj} fluctuate under the degradation of the gate oxide and features a small temperature dependence, making it a suitable aging precursor for condition monitoring. However, it is not possible to directly measure

[*1] Actual MOSFETs cannot be said to have no temperature dependence, because the ionization rate of the donor depends on the temperature. However, the temperature dependence of the C_{iss} is considered to be small, as described in Ref. [99]. Therefore, in this dissertation, the expression "the C_{iss} has a small temperature dependence" is used.

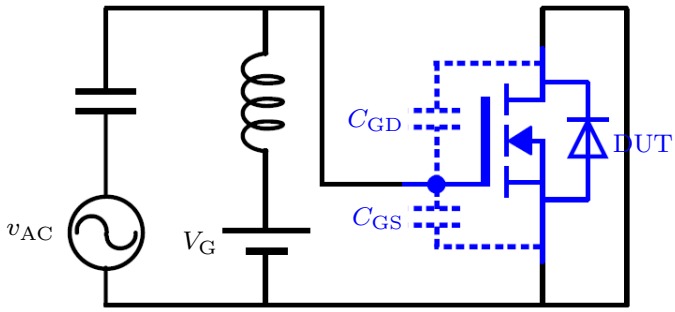


Fig.2.16. Circuit diagram for measuring the input capacitance C_{iss} of a MOSFET using the high-frequency method.

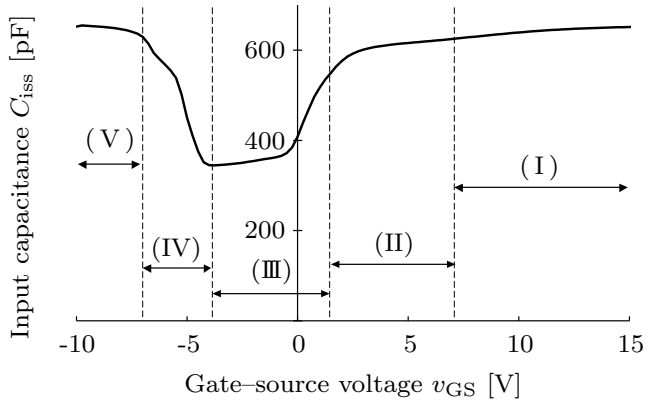


Fig.2.17. Measured C_{iss}–v_{GS} characteristics of a SiC MOSFET.

the depletion layer capacitance C_{dc}, C_{dj} in a packaged MOSFET.

One way to measure the depletion layer capacitance C_{dc}, C_{dj} of a packaged MOSFET is to measure the input capacitance C_{iss}, which is a voltage-dependent capacitance. The input capacitance C_{iss} is represented in the circuit diagram by the composite capacitance of the gate–source parasitic capacitance C_{GS} and the gate–drain parasitic capacitance C_{GD}. Fig. 2.16 shows a circuit diagram for measuring the input capacitance C_{iss} of a MOSFET using the high-frequency method. In this method, the drain–source of the DUT is shorted and the signal voltage v_{AC} is used to measure the voltage-dependent capacitance whilst the DC voltage V_G is applied to the gate–source. Details of the high-frequency measurement method are presented in Section 5.1.1.

Fig. 2.17 shows the measured input capacitance C_{iss} with respect to the gate–source voltage v_{GS} characteristic (C_{iss}–v_{GS} characteristic) of the SiC MOSFET

Table.2.2 MOSFET status and input capacitance C_{iss} at each section

Sec.	Channel region	JFET region	Input capacitance C_{iss}
(Ⅰ)	Inversion	Accumulation	$C_{\mathrm{oc}} + C_{\mathrm{oj}}$
(Ⅱ)	Depletion	Accumulation	$C_{\mathrm{oc}}C_{\mathrm{dc}}/\left(C_{\mathrm{oc}} + C_{\mathrm{dc}}\right) + C_{\mathrm{oj}}$
(Ⅲ)	Depletion	Depletion	$C_{\mathrm{oc}}C_{\mathrm{dc}}/\left(C_{\mathrm{oc}} + C_{\mathrm{dc}}\right) + C_{\mathrm{oj}}C_{\mathrm{dj}}/\left(C_{\mathrm{oj}} + C_{\mathrm{dj}}\right)$
(Ⅳ)	Accumulation	Depletion	$C_{\mathrm{oc}} + C_{\mathrm{oj}}C_{\mathrm{dj}}/\left(C_{\mathrm{oj}} + C_{\mathrm{dj}}\right)$
(Ⅴ)	Accumulation	Inversion	$C_{\mathrm{oc}} + C_{\mathrm{oj}}$

(C2M0280120D, Cree) used as the DUT in Section 4.3. The C_{iss}–v_{GS} characteristic was measured using a "high-voltage CV measurement system" (CS-603A, Iwatsu) at $v_{\mathrm{AC}} = 25$ mV and 1 MHz. As shown in Fig. 2.17, the input capacitance C_{iss} is the voltage-dependent capacitance. The C_{iss}–v_{GS} characteristic can be divided into five sections (Ⅰ)–(Ⅴ) depending on the parasitic capacitors shown in Fig. 2.15. Tab. 2.2 summarizes the state of the channel and JFET regions. In addition, the parasitic capacitors that make up the input capacitance C_{iss} at each section are summarized [17]. From Tab. 2.2, the input capacitance C_{iss} is composed of the oxide capacitances C_{oc} and C_{oj} and the depletion layer capacitances C_{dc} and C_{dj}.

Here, the oxide capacitances C_{oc} and C_{oj} are determined by the structure of the gate oxide, and they are independent of voltage and temperature. Therefore, the C_{iss}–v_{GS} characteristic fluctuates parallel to the v_{GS} axis as the oxide charge Q_{ox} changes along with the depletion layer capacitances C_{dc} and C_{dj}. Furthermore, the C_{iss}–v_{GS} characteristic has a small temperature dependence, in addition to the depletion layer capacitance C_{dc}, C_{dj}. Therefore, in packaged MOSFETs, the C_{iss}–v_{GS} characteristic represents a suitable aging precursor for condition monitoring. In this study, the C_{iss}–v_{GS} characteristic is proposed as an aging precursor for condition monitoring.

2.3 Summary

In this chapter, the current status of condition monitoring technology for power devices was introduced with reference to the relevant previous studies. The aging precursors proposed as condition monitoring techniques for power devices, as well

as their benefits and drawbacks, were summarized. It was shown that no unified aging precursor has thus far been defined. In addition, it was clarified that aging precursors that fluctuate with respect to gate oxide degradation and have a small temperature dependence are suitable for establishing the condition monitoring technology aimed at in this study.

In order to identify an aging precursor suitable for condition monitoring, the gate oxide degradation was theoretically investigated. It was theoretically shown that the electrical characteristics of power devices fluctuate depending on the oxide charge Q_{ox}. Furthermore, it was shown theoretically that the input capacitance C_{iss} (which is the voltage-dependent capacitor of the MOSFET) with respect to the gate–source voltage v_{GS} characteristic (C_{iss}–v_{GS} characteristic) fluctuates under changes in the oxide charge Q_{ox} and has a small temperature dependence. Therefore, in this study, the C_{iss}–v_{GS} characteristic is proposed as an aging precursor for condition monitoring.

Chapter 3

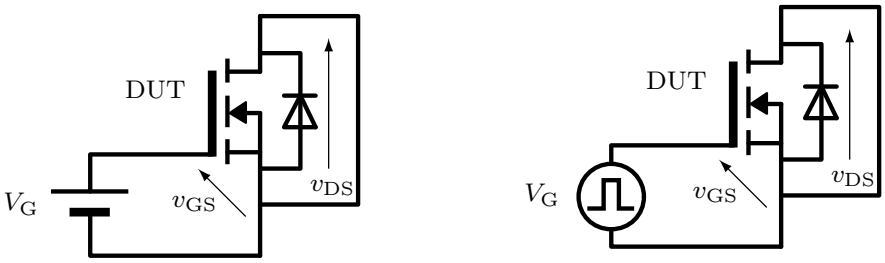
Accelerated Aging Test Circuit for Power Devices Applying Continuous Switching

In Section 2.2, the C_{iss}–v_{GS} characteristic is theoretically investigated as a suitable aging precursor for condition monitoring. In this chapter, an accelerated aging test circuit of the power device is developed, to experimentally verify the above theoretical investigation. To verify the degradation of power devices and thereby establish condition monitoring technology, it is necessary to perform accelerated aging tests under switching conditions similar to those of the power devices implemented in power conversion circuits. Therefore, a test circuit for accelerated aging under continuous switching conditions is proposed.

Based on analysis of the test circuit, a design method is proposed to ensure that no failures spread to that circuit, even when the DUT fails during the accelerated aging tests. The test circuit is designed according to the proposed method, and the experimental results at 500 V, 50 A or 800 V, 20 A conditions show the validity of the design method.

3.1 Review of Accelerated Aging for Power Devices

Power devices have a design lifetime of several decades. For this reason, accelerated aging tests are used to verify their degradation characteristics. These tests obtain the degradation characteristics within a realistic test time, by apply-



(a) DC stress voltage. (b) Square stress voltage.

Fig.3.1. Conventional HTGB test circuits.

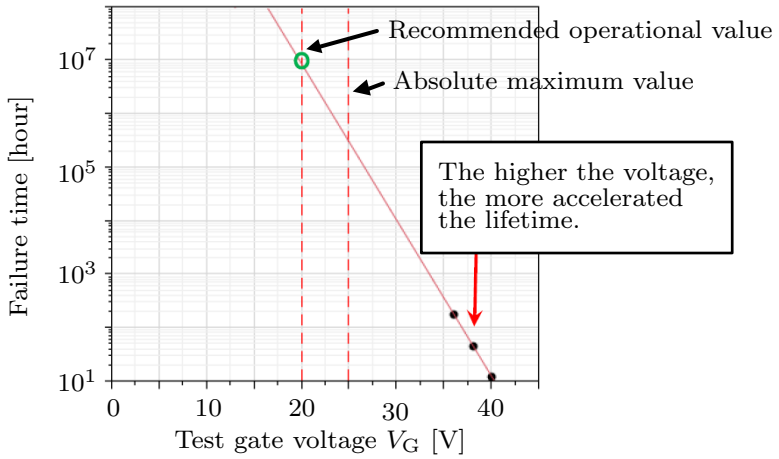


Fig.3.2. Lifetime evaluation of gate oxide using the conventional HTGB test [102].

ing intentionally higher voltages or temperatures than those normally used. This section provides a review of accelerated aging tests for power devices.

3.1.1 Stress on Gate Oxide

The HTGB test is generally used to induce accelerated aging in gate oxides. The HTGB test is defined as follows. "*The HTGB test biases the gate or other oxides of the device sample. The devices are normally operated in a static mode at (or near) the maximum rated oxide breakdown voltage levels*" [100]. Therefore, in conventional HTGB tests, a constant DC voltage is applied as a stress voltage at the gate–source of the DUT [101]. Fig. 3.1(a) shows the conventional HTGB test circuits. In the test circuit, the gate voltage V_G is set to an over-voltage, and the drain–source voltage v_{DS} is set to 0 V (shorted). Fig. 3.2 shows the result

of a conventional HTGB test conducted by a manufacturer on a SiC MOSFET [102]. The conventional HTGB test was performed with the test circuit shown in Fig. 3.1(a). As shown in Fig. 3.2, the higher the test gate voltage V_{G}, the more the lifetime is accelerated. Furthermore, the gate oxide lifetime at the recommended operational value can be estimated from the HTGB test result.

However, the gate oxide of SiC MOSFETs implemented in power conversion circuits receives stress under conditions different to those of the conventional HTGB test. Here, the stress applied to the gate oxide under switching conditions is considered.

Square Voltage

Under switching conditions, a square voltage is applied between the gate–source of the SiC MOSFET, instead of a constant DC voltage. Therefore, the square voltage is also used as the stress voltage for evaluating the gate oxide TDDB lifetime. Fig. 3.1(b) shows a test circuit that applies a square voltage as the stress voltage between the gate and source of the DUT. It has been reported that the gate oxide lifetimes of low-voltage MOSFETs (for LSIs) are longer when the square voltage is applied, compared to when DC voltage is applied [49][53][54][103]. However, there is a lack of HTGB test data for SiC MOSFETs when square voltage is applied as the stress voltage.

Drain–Source Voltage

The gate oxide is applied to the electrical field induced not only by the gate–source voltage v_{GS} but also by the drain–source voltage v_{DS}. The relationship between the drift layer field strength E_{dri} induced by the drain–source voltage v_{DS} and gate oxide field strength E_{ox} is given by [42]

$$E_{\mathrm{ox}} = \frac{\varepsilon_{\mathrm{s}}}{\varepsilon_{\mathrm{ox}}} E_{\mathrm{dri}}, \tag{3.1}$$

where $\varepsilon_{\mathrm{ox}}$ is the dielectric constant of the gate oxide. Because the maximum field strength of SiC is approximately ten times greater than that of Si, the maximum

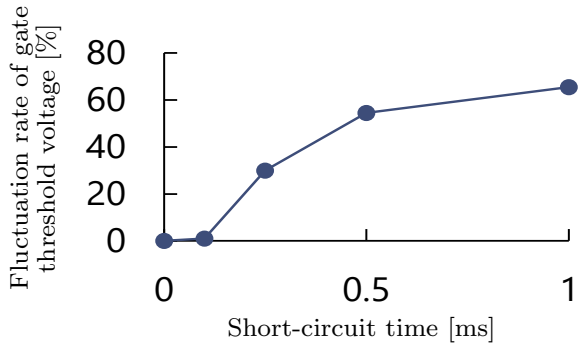


Fig.3.3. Short-circuit time and fluctuation rate of gate threshold voltage under repetitive short-circuit tests [43].

drift layer field strength of the SiC MOSFET can also be designed to be ten times greater than that of the Si MOSFET. Therefore, the gate oxide of SiC MOSFETs is more stressed by the drain–source voltage v_{DS} than that of Si MOSFETs.

Drain Current

Studies have reported gate oxide degradation attributable to localized heating of the gate oxide near the channel region by the drain current i_{D} [43]. In Ref. [43], repetitive short-circuit tests were performed upon SiC MOSFETs. Fig. 3.3 shows the relationship between the short-circuit time and fluctuation rate of the gate threshold voltage in the repeated short-circuit test. From Fig. 3.3, we see that the longer the short-circuit time, the larger the fluctuation rate of the gate threshold voltage. The reason for this is the localized heating of the gate oxide by the drain current i_{D}, as described above.

Under continuous switching conditions, these stresses are applied together as "dynamic-stress."

3.1.2 Accelerated Aging Applying Continuous Switching

A feature of conventional accelerated aging tests is that static stress is applied to accelerate the aging. Although the static-stress condition is effective in clarifying a specific cause of degradation, it is unsuitable for evaluating the dynamic stress applied under continuous switching conditions. The long-term reliability of Si power

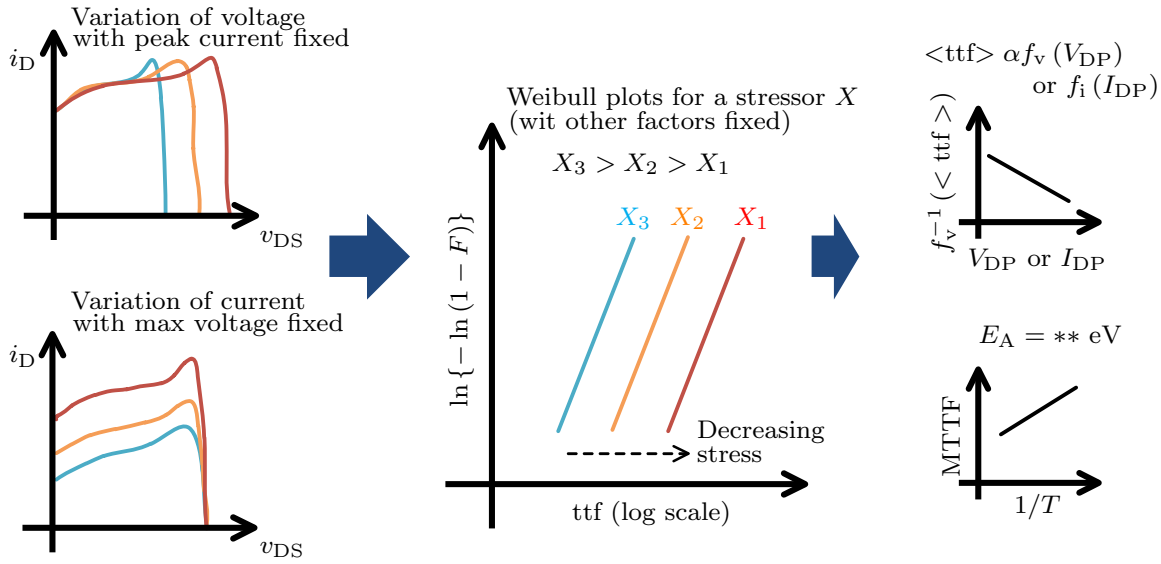


Fig.3.4. Overview of the method used to produce the wear model under the continuous switching accelerated aging test [104].

devices under dynamic stress has been achieved through years of experience and development [104]. Against this background, the Joint Electron Device Engineering Council (JEDEC) developed (in 2020) a standard that provides continuous switching tests for the long-term-reliability evaluation of gallium nitride (GaN) [104]. The purpose of the continuous switching test was to perform accelerated aging of wide bandgap power devices (which are less understood than Si power devices) under dynamic-stress conditions similar to those of actual use.

Fig. 3.4 presents an overview of the method used to obtain the wear model via the continuous switching accelerated aging test. In the test, the evaluation was based on the switching locus. For example, the test was performed with the maximum drain current i_D at a fixed value of I_{DP} and the maximum drain–source voltage v_{DS} at various values of V_{DP}. The maximum drain–source voltage V_{DP} was set higher than the normal operating voltage for accelerated aging, and the test was performed until the power devices failed. By calculating the failure time from the Weibull plot of the time to failure (ttf) for the power device at each V_{DP}, the mean time to failure (MTTF) can be expressed as a function of V_{DP}.

Fig. 3.5 presents an example of a continuous switching circuit shown in the

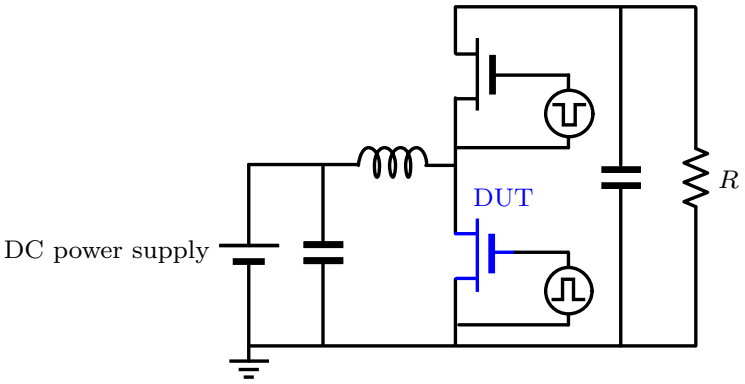


Fig.3.5. Example of a continuous switching circuit, as shown in the JEDEC standard [105].

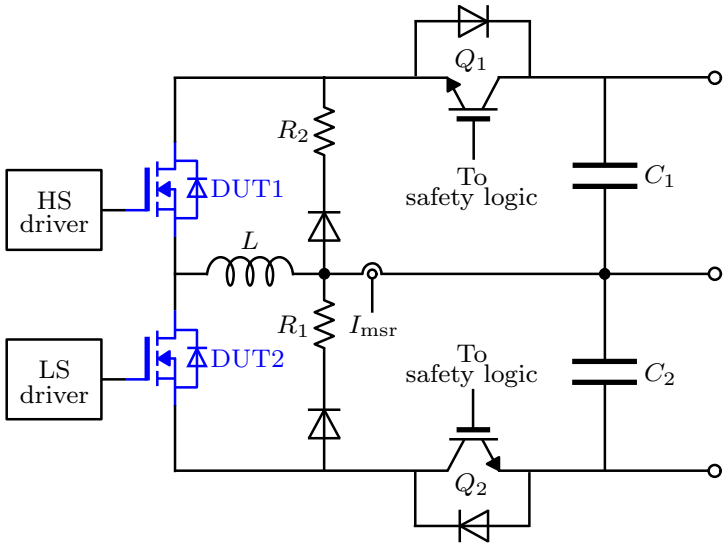
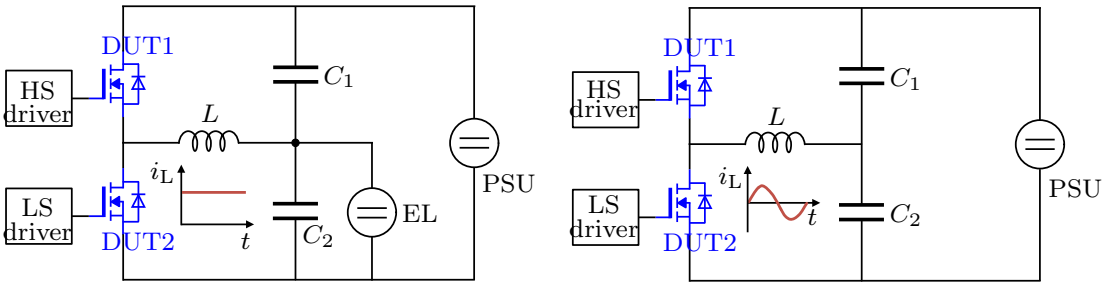


Fig.3.6. Continuous switching test circuit proposed in Ref. [106].

JEDEC standard. The circuit is composed of a boost converter and can perform accelerated aging tests for hard switching. However, because energy is consumed by a resistor R, a large-capacity DC power supply and resistor R are required when testing power devices with large capacities (e.g., power modules).

Ref. [106] proposed a circuit based upon a half-bridge inverter as a suitable test circuit for continuous switching tests. Fig. 3.6 shows the circuit diagram proposed in Ref. [106]. One feature of the circuit shown in Fig. 3.6 is that it is implemented with a protection circuit, assuming that the test is continued until the DUT fails. However, the protection circuit is implemented between the DC link capacitor and DUT (IGBT Q_1 and Q_2). This circuit configuration differs from that of a typical



(a) DC test current.

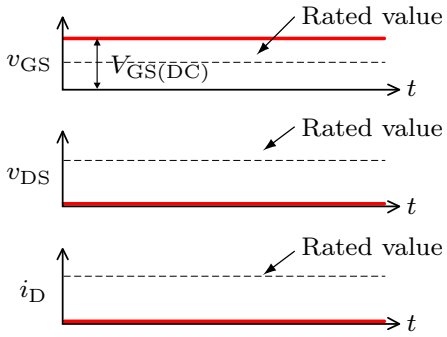
(b) AC test current.

Fig.3.7. Differences in load connections (attributable to test currents in the circuit) shown in Fig. 3.6.

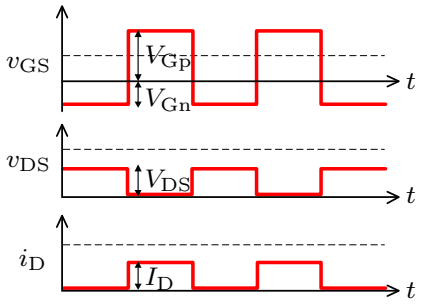
power conversion circuit. In addition, long-term reliability tests of power devices require test results from many samples. Therefore, multiple test circuits are used, and each test circuit must have a simple circuit configuration. Fig. 3.7 shows the difference in the loads connected between the DC and AC test currents in the test circuit shown in Fig. 3.6. When the test current is AC, the load is only the inductor L_1, and power regeneration is possible. On the other hand, when the load is DC, the load (EL) is connected. This resembles the test circuit shown in Fig. 3.5, where a large-capacity DC power supply (PSU) and load (EL) are required when testing power devices with large capacities (e.g., power modules).

Furthermore, there is no accelerated aging method and continuous-switching-operated test circuit for gate oxide. Therefore, to achieve the accelerated aging of SiC MOSFETs required in this study, the following issues should be solved:

- Consideration of a test method that facilitates accelerated aging of the gate oxide under continuous switching conditions
- Consideration of continuous switching circuits capable of power regeneration without a large power supply and load resistance



(a) Conventional HTGB test waveforms.



(b) Advanced HTGB test waveforms.

Fig.3.8. Accelerated aging test waveforms for conventional and advanced HTGB tests.

3.2 Overview of Proposed Test Method and Circuits

3.2.1 Proposed Advanced HTGB Test Method

An advanced HTGB test is proposed to accelerate the aging of the gate oxide under continuous switching conditions. The advanced HTGB test is a combination of the conventional HTGB test method and continuous switching test method established by the JEDEC standards [104][105].

Fig. 3.8(a) shows the conventional HTGB test waveforms. In the conventional HTGB test, a DC voltage V_G is applied to the gate–source of the DUT. The DC voltage V_G is set higher than the rated voltage, to produce accelerated aging of the gate oxide. Fig. 3.8(b) shows the test waveforms of the advanced HTGB test. As in the conventional HTGB test, the gate–source voltage V_{Gp} is set higher than the rated voltage. In addition, the test voltage V_{DS} and test current I_D are set to accelerate the gate oxide aging under continuous switching conditions. Therefore, the advanced HTGB test can evaluate the gate oxide degradation under conditions resembling the actual operating conditions. It should be noted that the advanced HTGB test is proposed not to accurately evaluate the relationship between the gate oxide bias and degradation but to induce accelerated aging of the gate oxide

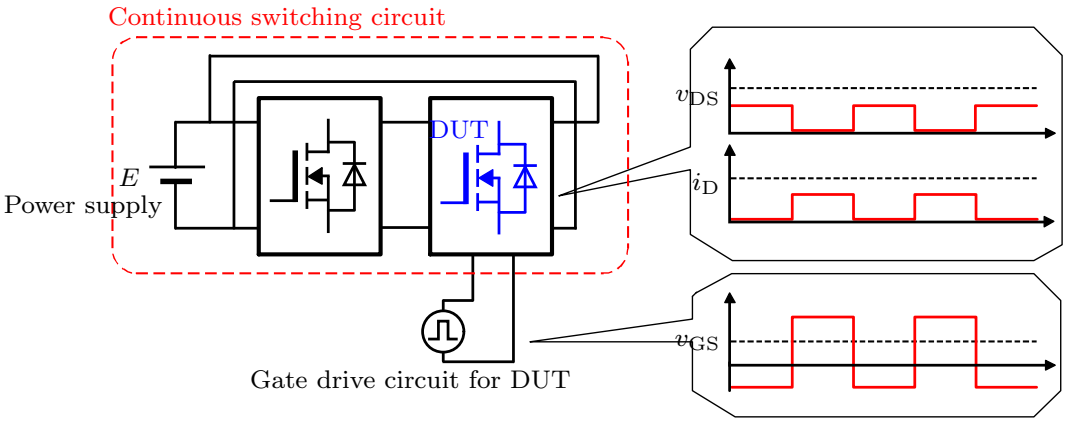


Fig.3.9. Schematic diagram of advanced HTBG test circuit.

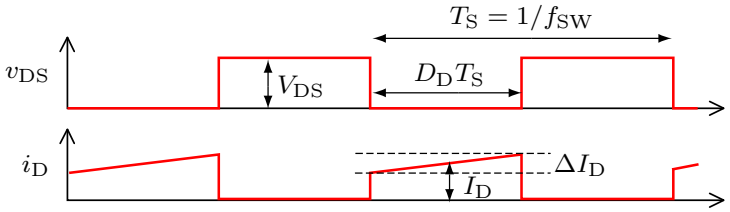


Fig.3.10. Ideal waveforms of general hard switching.

under conditions similar to the actual operating conditions.

3.2.2 Advanced HTGB Test Circuit Specifications

A test circuit was developed to perform the advanced THGB test. Fig. 3.9 shows a schematic diagram of the advanced HTGB test circuit; it consists of a continuous switching circuit and gate drive circuit for the DUT. In this chapter, the continuous switching circuit and gate drive circuit for the DUT were developed separately. The target switching waveform to be developed is that of hard switching, which is commonly applied in power conversion circuits. Fig. 3.10 depicts the ideal switching waveform of hard switching. In Fig. 3.10, V_{DS} is the test voltage, I_D is the test current, D_D is the on-duty ratio of the DUT, f_{SW} is the switching frequency, T_S is the switching period, and ΔI_D is the current ripple of the test current I_D. The following conditions are required for the test circuit specified in the JEDEC standards [104]:

- To set the test voltage V_{DS} higher than the normal operating voltage for accelerated aging, it should be adjustable according to the test conditions within a range extending up to the maximum rated voltage of the DUT.
- To set the test current I_{D} larger than the normal operating current for accelerated aging, it should be adjustable according to the test conditions within a range extending up to the maximum rated current of the DUT.
- The switching frequency f_{SW} should be adjustable according to the test conditions.
- The on-duty ratio D_{D} should be adjustable according to the test conditions.
- The test should be able to run until the DUT fails.

The specifications of the continuous switching circuit should satisfy these conditions and be able to solve the issues described in Section 3.2.1.

3.2.3 Existing Power Supply System and Circuit Configuration

To achieve continuous switching operation and power regeneration, a cascaded buck-boost (or boost-buck) converter is adopted as the continuous switching circuit. Furthermore, because the load current of the circuit is DC, the test current I_{D} is constant and therefore suitable for continuous switching tests.

In continuous switching tests (unlike switching tests), the energy consumed during the continuous test must be supplied from a DC power supply. A DC power supply with a large voltage rating and large capacity is required for testing power modules with large voltages and current ratings [107, 108]. Hence, two types of continuous switching circuits are proposed for testing DUTs of various voltage and current ratings: The first type is the cascaded buck-boost converter, which is hereafter referred to as the "buck-type test circuit." The buck-type test circuit can be used only when the test voltage V_{DS} is lower than the output voltage of the DC power supply. The second type is the cascaded boost-buck converter, hereinafter

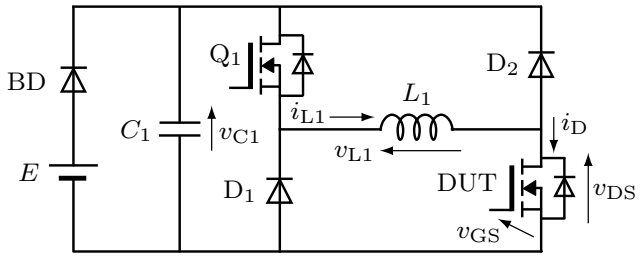


Fig.3.11. Circuit diagram of buck-type test circuit.

referred to as the "boost-type test circuit." The boost-type test circuit can boost the input voltage and be set to a test voltage V_{DS} that exceeds the output voltage of the DC power supply. In this dissertation, each design method is proposed. By considering the design method, it is shown that the buck-type test circuit is more suitable when the test voltage V_{DS} is lower than the output voltage of the existing DC power supply. On the other hand, in long-term reliability tests of power devices, and depending on the test conditions, the DUT is operated near its rated voltage for accelerated aging. Therefore, when a test voltage V_{DS} exceeding the output voltage of the existing DC power supply is required, the boost-type test circuit is suitable.

3.3 Design of Buck-type Test Circuit

Fig. 3.11 shows the circuit diagram of the buck-type test circuit [109]. The buck and boost converters are connected in this order from a DC power supply side, and the output of the boost converter is connected to the input of the buck converter to realize power regeneration. The DUT is implemented as a transistor of the boost converter because it acts as a low-side transistor, which is suitable for measurement. A diode BD is inserted to prevent a voltage exceeding the input voltage from being applied to the DC power supply. As shown in Fig. 3.11, the inductor of the buck converter and boost converter can be shared [110].

In this dissertation, when the DUT fails, we refer to it as "abnormal operation." Meanwhile, we use "normal operation" to refer to failure during the continuous

TABLE.3.1 OPERATING MODES OF BUCK-TYPE TEST CIRCUIT.

Operating mode	Q_1	DUT	v_{L1}
A	ON	ON	E
B	ON	OFF	0
C	OFF	ON	0
D	OFF	OFF	$-E$

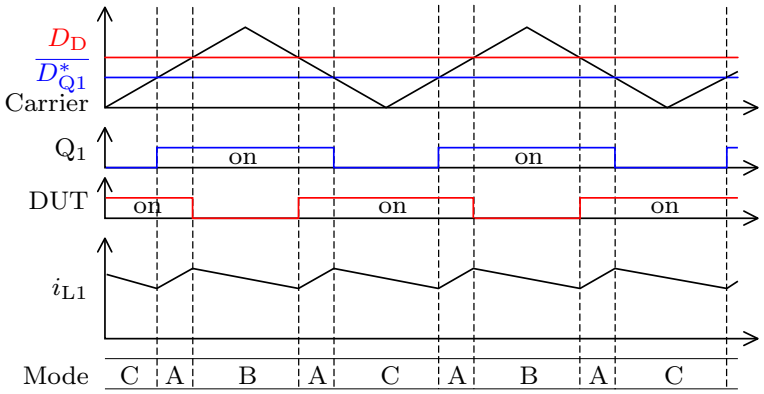


Fig.3.12. Theoretical gate waveform and inductor current waveform of the buck-type test circuit.

switching test. A control method for the test voltage V_{DS} and test current I_D during normal operation is described below. In addition, because the circuit parameters are dominated by the influence of an overvoltage or overcurrent during abnormal operation, the circuit parameter design method that considers abnormal operation is described.

3.3.1 Control Method for Normal Operation

Because the test voltage V_{DS} is equal to the input voltage E, it can be set arbitrarily by the DC power supply, as shown in the following equation:

$$V_{DS} = E. \tag{3.2}$$

The inductor current i_{L1} is feedback-controlled by a transistor Q_1 of the buck converter to arbitrarily set the test current I_D. However, the volume of the inductor should be largely produced by the DC current I_D that constantly flows through the inductor. Therefore, a control method that can reduce the current ripple ΔI_D is applied to reduce the inductance L_1.

The circuit operation can be divided into four modes according to the on/off

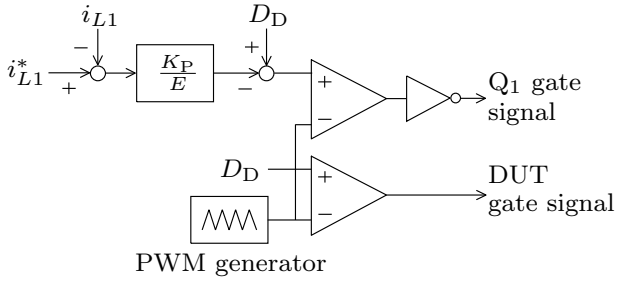


Fig.3.13. Control block diagram.

state of the transistor Q_1 and the DUT. Tab. 3.1 shows an inductor voltage $v_{\rm L1}$ in the four modes. Even in Modes B and C, the inductor current $i_{\rm L1}$ decreases because of the power loss in the circuit. Therefore, Mode A occurs, and energy is supplied to the inductor. Fig. 3.12 shows the gate waveforms and inductor current $i_{\rm L1}$ waveform, using only Modes A, B, and C. The off-duty ratio command value $\overline{D^*_{\rm Q1}}$ of the transistor Q_1 is represented as [111]

$$\overline{D^*_{\rm Q1}} = D_{\rm D} - \frac{K_{\rm P}}{E}\left(i^*_{\rm L1} - i_{\rm L1}\right), \tag{3.3}$$

where $K_{\rm P}$ is the proportional gain, and $i^*_{\rm L1}$ is the inductor current command value, which is equal to the test current $I_{\rm D}$. Fig. 3.13 shows the control block diagram.

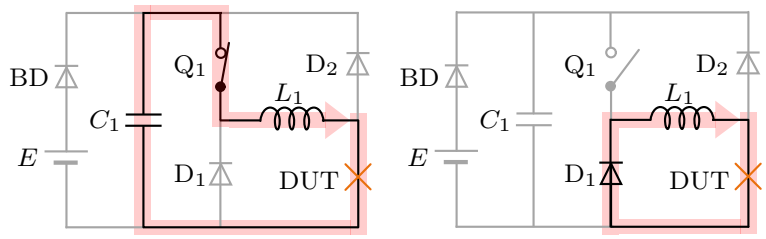
The ratio $d_{\rm A}$ in Mode A is a single period, given by

$$d_{\rm A} = \frac{I_{\rm D}}{E - \left(R_{\rm Q1} - R_{\rm D1}\right) I_{\rm D}} \times \left\{\left(-R_{\rm Q1} + R_{\rm DUT} + R_{\rm D1} - R_{\rm D2}\right) D_{\rm D} + R_{\rm Q1} + R_{\rm D2} + R_{\rm L1}\right\}, \tag{3.4}$$

where $R_{\rm Q1}$, $R_{\rm DUT}$, $R_{\rm D1}$, $R_{\rm D2}$, and $R_{\rm L1}$ are the resistances of Q_1, DUT, D_1, D_2, and L_1, respectively.

When the control method described above is applied, the current ripple $\Delta I_{\rm D}$ during normal operation is given by the following equation:

$$\Delta I_{\rm D} = \frac{\left(R_{\rm Q1} + R_{\rm D2} + R_{\rm L}\right) I_{\rm D}}{L_1}\left(1 - D_{\rm D}\right) T_{\rm S}. \tag{3.5}$$



(a) Q_1 is ON (b) Q_1 is OFF

Fig.3.14. Equivalent circuit of the buck-type test circuit when a short circuit occurs in the DUT.

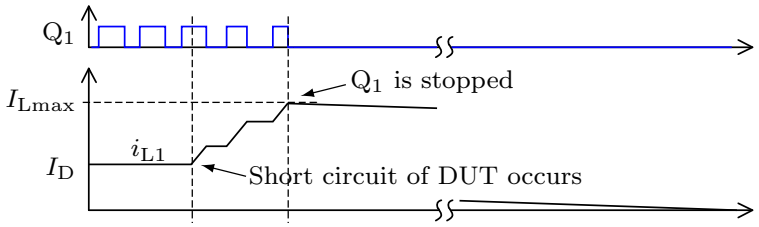


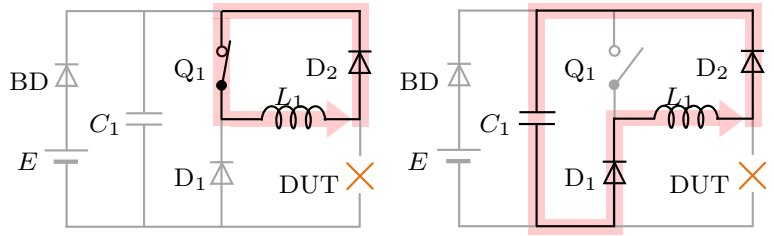
Fig.3.15. Theoretical gate waveform and inductor current waveform when a short circuit occurs in the DUT.

3.3.2 Circuit Parameter Design Considering Abnormal Operation

The circuit operation when the DUT is short-circuited or open during the continuous switching test (i.e., abnormal operation) is analyzed. This occurs because both short-circuit and open failures of the DUT can arise in accelerated aging tests for gate oxides. If the gate oxide TDDB occurs during the accelerated aging test, the DUT will undergo a short circuit failure. If a BTI-induced increase in gate threshold voltage occurs during the accelerated aging test, the DUT will register an open failure. In addition, the inductor and capacitor design method considered in the analysis results is shown.

Design of Inductor

Fig. 3.14 depicts the equivalent circuit when a short circuit of the DUT occurs. When the transistor Q_1 is on, the inductor current i_{L1} increases owing to the inductor voltage $v_{L1} = E$. When transistor Q_1 is off, the inductor current i_{L1} is freewheeling in the circuit. Fig. 3.15 depicts the inductor current i_{L1} when a short



(a) Q$_1$ is ON (b) Q$_1$ is OFF

Fig.3.16. Equivalent circuit of the buck-type test circuit when open failure of DUT occurs.

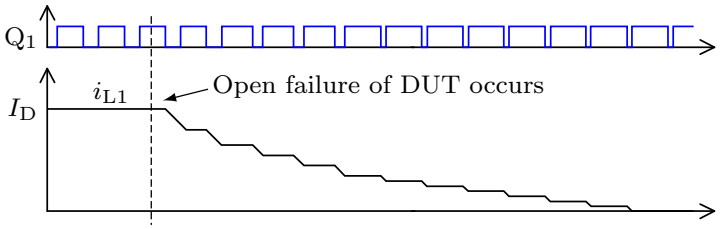


Fig.3.17. Theoretical gate waveform and inductor current waveform when open failure of the DUT occurs.

circuit occurs in the DUT. In the event of a DUT short-circuiting, the inductor current i_{L1} increases and exceeds the value of the test current I_D. Therefore, the operation of the transistor Q$_1$ should be stopped by detecting an overcurrent of the inductor current i_{L1}. The maximum value of the inductor current I_{Lmax} is given by

$$I_{Lmax} = I_D + \frac{E}{L_1} T_{ON}, \tag{3.6}$$

where T_{ON} is the total on-time of the transistor Q$_1$ between the time when the short circuit of the DUT occurs and the time when the transistor Q$_1$ is stopped. In Eq. 3.6, the resistance components in the test circuit were neglected when considering the worst case. As the total on-time T_{ON} depends on the switching frequency f_{SW} and the delay time for overcurrent detection, it is necessary to design the inductance L_1 by considering this.

Design of Capacitor

The design of the capacitor should account for the open failure of the DUT. Fig. 3.16 illustrates the equivalent circuit when this open failure occurs. When

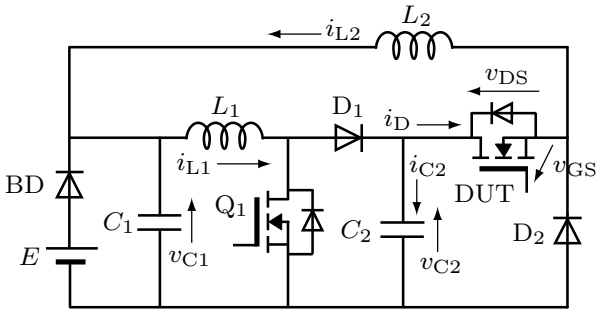


Fig.3.18. Circuit diagram of the boost-type test circuit.

transistor Q_1 is on, the inductor current i_{L1} is freewheeling in the circuit. When transistor Q_1 is off, the inductor current i_{L1} decreases owing to the inductor voltage $v_{L1} = -E$. Fig. 3.17 shows the inductor current i_{L1} at open failure. In the event of a DUT open failure, the inductor current i_{L1} decreases and gradually reaches 0 A. However, because the energy of the inductor is transferred to the capacitor, the capacitor voltage v_{C1} increases and exceeds the input voltage E. The maximum value of the capacitor voltage V_{Cmax} is given by the following equation:

$$V_{Cmax} = \sqrt{\frac{L_1}{C_1} I_D^2 + E^2}. \tag{3.7}$$

In Eq. 3.7, the resistance components in the test circuit were neglected when considering the worst case.

3.4 Design of Boost-type Test Circuit

Fig. 3.18 depicts the circuit diagram of the boost-type test circuit. The boost and buck converters were connected in this order from the DC power supply side. The output of the buck converter was connected to the input of the boost converter to realize power regeneration. The DUT was implemented as a transistor for the buck converter. When the transistor of the boost converter was the DUT, short-circuiting of the DUT occurred, and a short circuit occurred in the DC power supply via the inductor L_1. This short circuit of the DC power supply cannot be stopped by the transistor of the buck converter. Therefore, the DUT should perform the role of this transistor.

TABLE.3.2 OPERATING MODES OF THE BOOST-TYPE TEST CIRCUIT.

Operating mode	Q_1	DUT	i_{C2}
A	ON	ON	$-i_{L2}$
B	ON	OFF	0
C	OFF	ON	0
D	OFF	OFF	i_{L2}

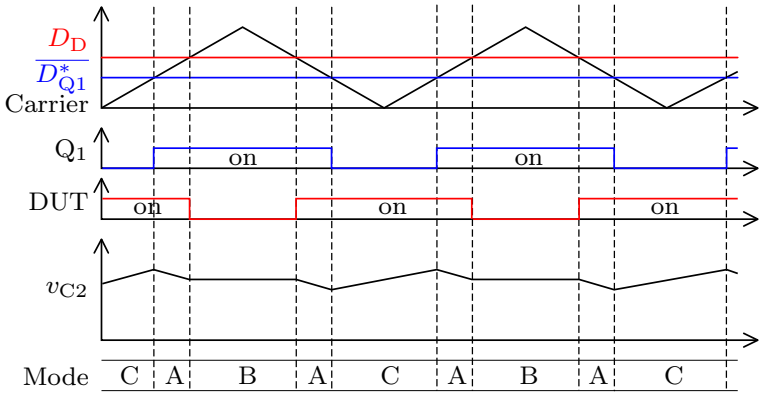


Fig.3.19. Theoretical gate waveform and capacitor voltage waveform of the boost-type test circuit.

The control method for the test voltage V_{DS} and test current I_D during normal operation is described below. In addition, because the circuit parameters are dominated by the influence of an overvoltage or overcurrent during abnormal operation, the circuit parameter design method that considers abnormal operation is described.

3.4.1 Control Method for Normal Operation

The test voltage V_{DS} is bucked to the input voltage E by a buck converter with a duty ratio of D_D. Therefore, the test voltage V_{DS} is given by the following equation:

$$V_{DS} = \frac{E}{D_D}. \tag{3.8}$$

An inductor current i_{L1} is feedback-controlled by a transistor Q_1 of the boost converter, to set the test current I_D arbitrarily. No limitations are placed on the set value of the test voltage V_{DS}; thus, theoretically, the design limits of the test voltage V_{DS} are small. However, because it is necessary to select a capacitor with

a high rated voltage, film capacitors should be applied. When the test current I_{D} flows through capacitor C_2, the voltage ripple tends to increase. Therefore, the control method described below was applied to reduce the capacitance C_2.

The circuit operation can be divided into four modes according to the on/off state of the transistor Q_1 and the DUT. Tab. 3.2 shows the capacitor current i_{C2} in the four modes. Even in Mode C, the capacitor voltage v_{C2} increases because the energy corresponding to the loss of the buck converter is provided from the DC power supply. Therefore, Mode A occurs, and capacitor C_2 supplies energy to the buck converter. Fig. 3.19 shows the gate waveforms and capacitor voltage v_{C2} waveform, using only Modes A, B, and C. The off-duty ratio command value $\overline{D^*_{\mathrm{Q1}}}$ of the transistor Q_1 is as follows:

$$\overline{D^*_{\mathrm{Q1}}} = D_{\mathrm{D}} - \frac{K_{\mathrm{P}}}{E}\left(i^*_{\mathrm{L1}} - i_{\mathrm{L1}}\right). \tag{3.9}$$

The control block diagram matches that of the buck-type test circuit shown in Fig. 3.13.

The ratio d_{A} in which Mode A occurs is a single period, which is given by

$$d_{\mathrm{A}} = \frac{E + \left(2R'' - R'''\right) I_{\mathrm{D}} - \sqrt{\alpha}}{2\left(E + R'' I_{\mathrm{D}}\right)} D_{\mathrm{D}}, \tag{3.10}$$

where

$$\alpha = \left\{E + \left(2R'' - R'''\right) I_{\mathrm{D}}\right\}^2 D_{\mathrm{D}}^2 - 4\left(E + R'' I_{\mathrm{D}}\right)\left(R' + R''\right) I_{\mathrm{D}} D_{\mathrm{D}}^2, \tag{3.11}$$

$$R' = R_{\mathrm{L1}} + R_{\mathrm{Q1}}\left(1 - D_{\mathrm{D}}\right) + R_{\mathrm{D1}} D_{\mathrm{D}}, \tag{3.12}$$

$$R'' = R_{\mathrm{L2}} + R_{\mathrm{DUT}} D_{\mathrm{D}} + R_{\mathrm{D2}}\left(1 - D_{\mathrm{D}}\right), \tag{3.13}$$

$$R''' = \left(R_{\mathrm{Q1}} - R_{\mathrm{D1}}\right) D_{\mathrm{D}}, \tag{3.14}$$

where R_{L2} is a resistance of L_2.

3.4.2 Circuit Parameter Design Considering Abnormal Operation

In the boost-type test circuit, when short-circuiting of the DUT occurs during the continuous switching test, a maximum current I_{Lmax} that exceeds the test current

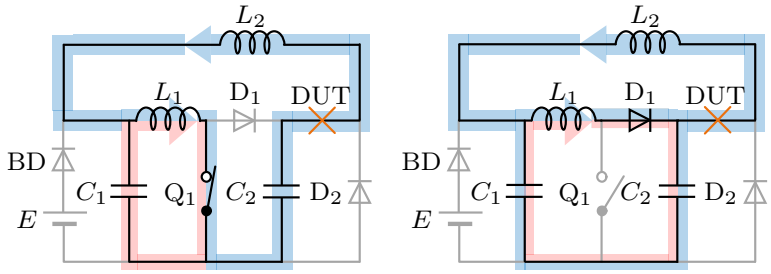


Fig.3.20. Equivalent circuit of the boost-type test circuit when short circuiting of the DUT occurs.

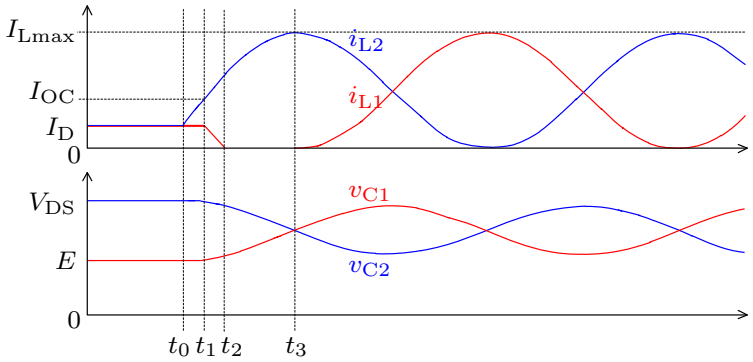


Fig.3.21. Theoretical waveforms when short circuiting of the DUT occurs.

I_D occurs. In addition, when an open failure of the DUT occurs, a maximum voltage V_{Cmax} that exceeds the test voltage V_{DS} occurs. Thus, the abnormal operation is analyzed, and the maximum current I_{Lmax} and maximum voltage V_{Cmax} are calculated. Moreover, a relationship between the abnormal operation, inductance, and capacitance is shown, to help design inductors and capacitors.

In this section, the inductances L_1 and L_2 and capacitances C_1 and C_2 satisfy the following equations because the maximum current I_{Lmax} and maximum voltage V_{Cmax} are minimized under the following conditions:

$$L_1 = L_2 = L, \tag{3.15}$$

$$C_1 = C_2 = C. \tag{3.16}$$

Furthermore, in the abnormal operation analysis, the resistance components in the test circuit are neglected, to consider the worst case.

Short Circuit Failure of DUT

Fig. 3.20 shows the equivalent circuit when a short circuit of the DUT occurs. Fig. 3.21 shows the theoretical waveforms when the short circuit occurs. In Fig. 3.21, a short circuit occurs at time $t = t_0$. In the period t_0-t_1, the inductor current i_{L2} increases owing to the capacitor voltage $v_{C1} < v_{C2}$. The inductor current $i_{L1} = I_D$, owing to the constant current control. Therefore, an overcurrent I_{OC} of the inductor current i_{L2} should be detectable. At time $t = t_1$, the operation of the transistor Q_1 is halted by the overcurrent I_{OC} of the inductor current i_{L2}. After $t = t_1$, it can be divided into two patterns, depending on the inductor current i_{L1}. One pattern is the inductor current, i_{L1}, in the continuous conduction mode; the other pattern is the inductor current i_{L1} in a discontinuous conduction mode for $t = t_2 - t_3$, as shown in Fig. 3.21.

When the inductor current i_{L1} is in the continuous conduction mode, the minimum value I_{Lmin} of the inductor current i_{L1} satisfies

$$I_{Lmin} \simeq I_D + I_{OC} - \sqrt{\frac{C}{L}\left(1 - D_D\right)^2 V_{DS}^2 + \left(I_D - I_{OC}\right)^2} > 0, \tag{3.17}$$

and the maximum current I_{Lmax} is given by the following equation:

$$I_{Lmax} \simeq \frac{1}{2}\left(I_D + I_{OC}\right) + \frac{1}{2}\sqrt{\frac{C}{L}\left(1 - D_D\right)^2 V_{DS}^2 + \left(I_D - I_{OC}\right)^2}. \tag{3.18}$$

The approximate expressions $v_{C2}(t_1) \simeq V_{DS}$ and $v_{C1}(t_1) \simeq E_1 = D_D V_{DS}$ are applied to Eq. 3.17 and Eq. 3.18.

When $I_{Lmin} \leq 0$, the inductor current i_{L1} reaches 0 A at time $t = t_2$. In the period t_2-t_3, the inductor current $i_{L1} = 0$ A because the diode D_1 is off. At time $t = t_3$, the inductor current i_{L2} reaches the maximum current I_{Lmax}, which is given by

$$I_{Lmax} \simeq \sqrt{\frac{C}{2L}\left(1 - D_D\right)^2 V_{DS}^2 + \left(I_D + I_{OC}\right)^2}. \tag{3.19}$$

The approximate expressions $v_{C2}(t_2) \simeq V_{DS}$ and $v_{C1}(t_2) \simeq E_1 = D_D V_{DS}$ are applied to Eq. 3.19.

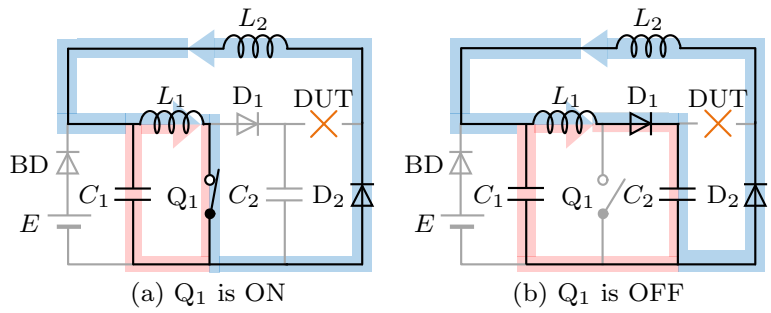


Fig.3.22. Equivalent circuit of the boost-type test circuit when open failure of the DUT occurs.

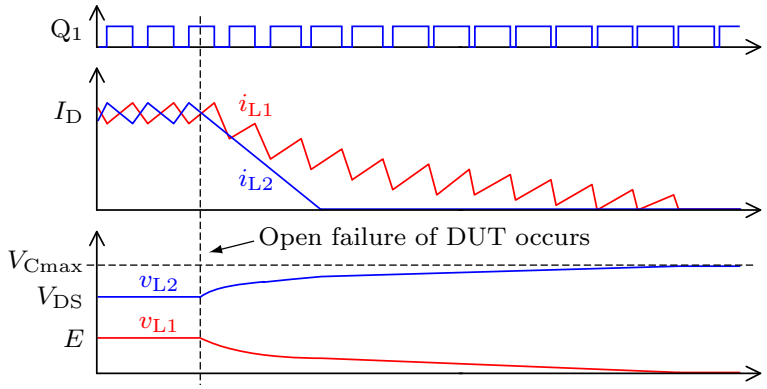


Fig.3.23. Theoretical waveforms when open failure of the DUT occurs.

Open Failure of DUT

Fig. 3.22 depicts the equivalent circuit when open failure of the DUT occurs. Similarly, Fig. 3.23 shows the theoretical gate, inductor current, and capacitor voltage waveforms under such failure. The inductor currents i_{L1} and i_{L2} and capacitor voltage v_{C1} gradually decrease because their energy is transferred to the capacitor C_2. Thus, the capacitor voltage v_{C2} increases, and its maximum value V_{Cmax} is given by the following equation:

$$V_{Cmax} = \sqrt{\frac{2L}{C} I_D^2 + V_{DS}^2 + E^2}. \tag{3.20}$$

3.4.3 Design of Inductor and Capacitor

From Eqs. 3.18–3.20, the maximum voltage V_{Cmax} and maximum current I_{Lmax} are seen to depend on the ratio of inductance L and capacitance C (thus L/C). Fig. 3.24 illustrates the calculation and circuit simulation results of V_{Cmax} and

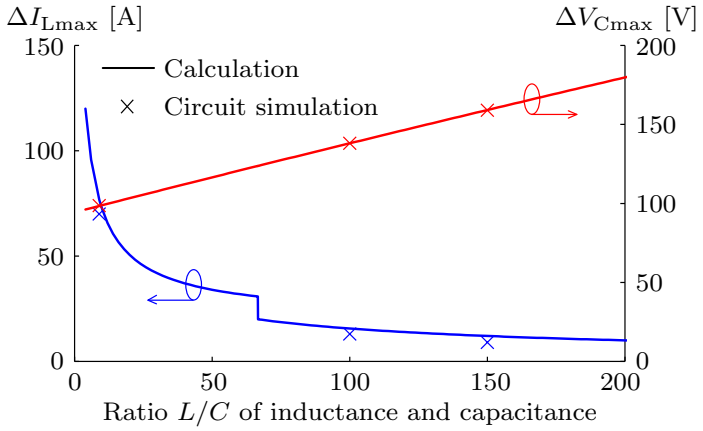


Fig.3.24. Calculation and simulation results of ΔV_{Cmax} and ΔI_{Lmax}.

TABLE.3.3 CALCULATION AND SIMULATION CONDITIONS OF THE BOOST-TYPE TEST CIRCUIT.

Parameters	Value
Test voltage V_{DS}	800 V
Test current I_{D}	20 A
Duty ratio of DUT	0.5
Overcurrent detection value I_{OC}	30 A

I_{Lmax}. The calculation and circuit simulation conditions are listed in Tab. 3.3. In Fig. 3.24, ΔV_{Cmax} and ΔI_{Lmax} are defined by the following equations:

$$\Delta V_{\mathrm{Cmax}} = V_{\mathrm{Cmax}} - V_{\mathrm{DS}}, \tag{3.21}$$

$$\Delta I_{\mathrm{Lmax}} = I_{\mathrm{Lmax}} - I_{\mathrm{OC}}. \tag{3.22}$$

In Eqs. 3.18 and 3.19, even though the approximation is used, the calculated results almost replicate the circuit simulation results. As V_{Cmax} and I_{Lmax} exist in a trade-off relationship, it is necessary to design L/C by considering both.

During normal operation, because the current ripple ΔI_{D} is equivalent to the current ripple of the inductor current i_{L2}, it is given by the following equation:

$$\Delta I_{\mathrm{D}} = \frac{\{(R_{\mathrm{L2}} + R_{\mathrm{D2}})\, I_{\mathrm{D}} + E\}\,(1 - D_{\mathrm{D}})}{L_2 f_{\mathrm{SW}}}. \tag{3.23}$$

From the above equations and the relationship of Fig. 3.24, the inductance L and capacitance C can be designed.

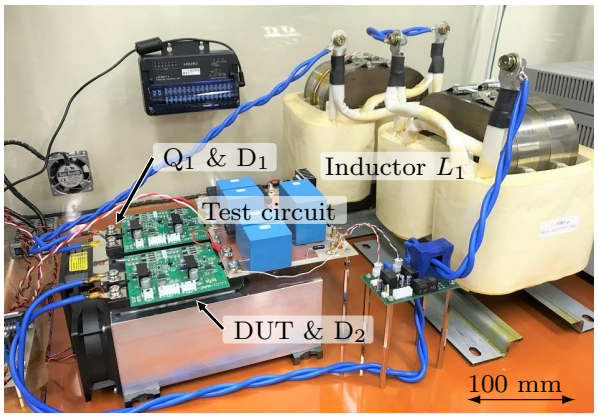


Fig.3.25. Experimental setup of test circuit.

TABLE.3.4 CIRCUIT PARAMETERS OF BOTH BUCK-TYPE AND BOOST-TYPE TEST CIRCUIT.

Parameters	Value of buck-type	Value of boost-type
Capacitance	$C_1 = 80\ \mu$F	$C_1 = C_2 = 40\ \mu$F
Inductance	$L_1 = 740\ \mu$H	$L_1 = L_2 = 370\ \mu$H
Resistance	$R_{\mathrm{L1}} = 20\ \mathrm{m}\Omega$	$R_{\mathrm{L1}} = R_{\mathrm{L2}} = 10\ \mathrm{m}\Omega$
Resistance	$R_{\mathrm{Q1}} = R_{\mathrm{DUT}} = 25\ \mathrm{m}\Omega$ [112]	
Resistance	R_{D1}=$R_{\mathrm{D2}} = 30\ \mathrm{m}\Omega$ [112]	

TABLE.3.5 SPECIFICATIONS OF POWER DEVICES.

Contents	Value
Type number	BSM120D12P2C005 (ROHM)
Rated drain-source voltage	1,200 V
Rated drain current	134 A
Rated gate-source voltage	+22/−6 V

TABLE.3.6 SPECIFICATIONS OF MEASURING INSTRUMENTS.

Measuring instruments	Manufacturer	Model number	Specifications	Measurement points
Oscilloscope	Iwatsu	DS-5634A	350 MHz, 1 GS/s	−
Differential probe	Iwatsu	SS-320	100 MHz	v_{DS}, v_{GS}
Rogowski coil	Iwatsu	SS-664	32−30 MHz, 300 A	i_{D}
Current probe	Iwatsu	SS-260	10 MH, 150 A	i_{L1}, i_{L2}

3.5 Experimental Verification of Buck/Boost Type Test Circuits

Experiments were performed to validate the design methods described in Sections 3.3 and 3.4. Fig. 3.25 shows the experimental setup of the test circuit. Tab. 3.4 shows the circuit parameters of both the buck and boost-type test circuits. The

Table.3.7 Experimental conditions of the buck-type test circuit.

Contents	Value
Test voltage V_{DS}	500 V
Test current I_{D}	50 A
Switching frequency f_{SW}	100 kHz
Duty ratio of DUT D_{D}	0.5
Overcurrent detection value I_{OC}	70 A

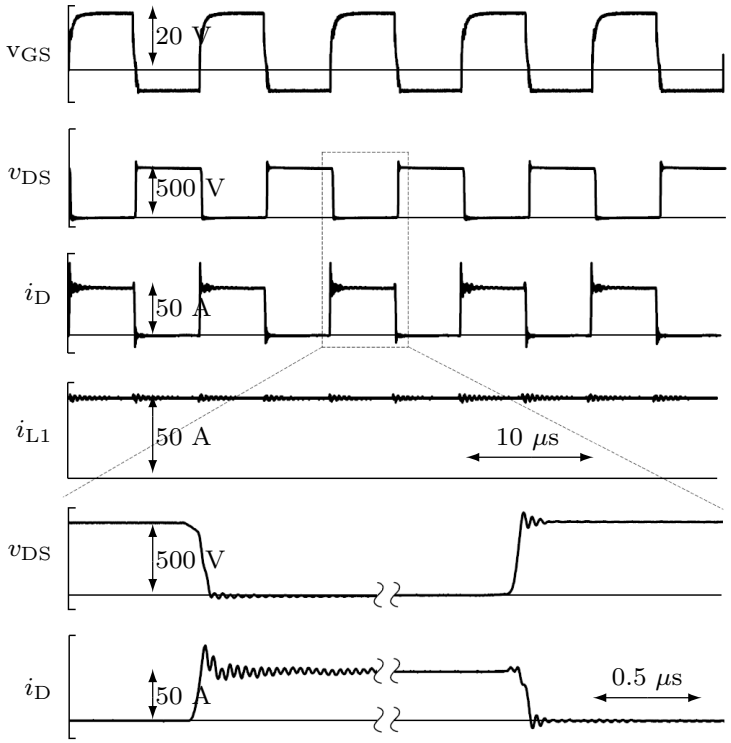


Fig.3.26. Experimental waveforms of buck-type test circuit.

test circuit can be switched between a buck- or boost-type test circuit by changing the wiring. The boost-type test circuit requires two capacitors and inductors. These two capacitors were arranged in parallel and the inductors were arranged in series in the buck-type test circuit; hence, both the capacitance and inductance were twice as high as those in the boost-type test circuit. Tab. 3.5 shows the specifications of the power devices used in the experiment. To verify the operation of the test circuit, the same devices were used for transistors Q_1 and the DUT. The proportional gain K_{P} was set to 5.0 [113]. Tab. 3.6 shows the specifications of the measuring instruments used in the experiment.

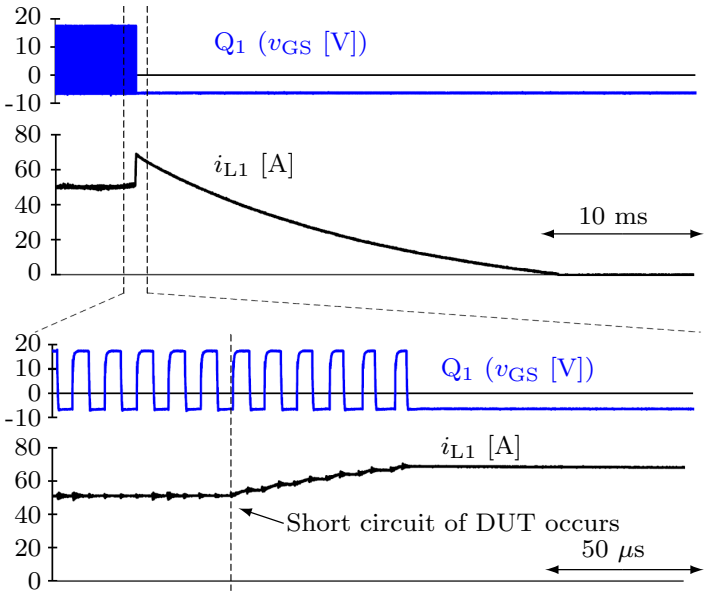


Fig.3.27. Experimental gate waveform and inductor current waveform when short circuit of the DUT occurs.

3.5.1 Buck-type Test Circuit

Tab. 3.7 shows the experimental conditions for the buck-type test circuit. The test voltage V_{DS} was set to 500 V, which is the rated voltage of the DC power supply. The test current I_{D} was set to 50 A. Under these conditions, the conversion capacity was 12.5 kW because the duty ratio of the DUT was set to 0.5.

Fig. 3.26 depicts the experiment waveforms during normal operations. Because the test current I_{D} was measured by a Rogowski coil, the DC component was offset in Fig. 3.26. Almost no current ripple ΔI_{D} was observed, because the control method described in Section 3.3.1 was applied. The input power of the DC power supply was 610 W, which was 4.9% of the conversion capacity.

Fig. 3.27 shows the experimental waveforms when short-circuiting of the DUT occurs. The overcurrent detection value of the inductor current i_{L1} was set to 70 A. The transistor Q_1 stopped operating owing to the detection of an overcurrent. In addition, the inductor current i_{L1} gradually decreased and reached 0 A. Thus, the test can be stopped without spreading the DUT failure to the test circuit.

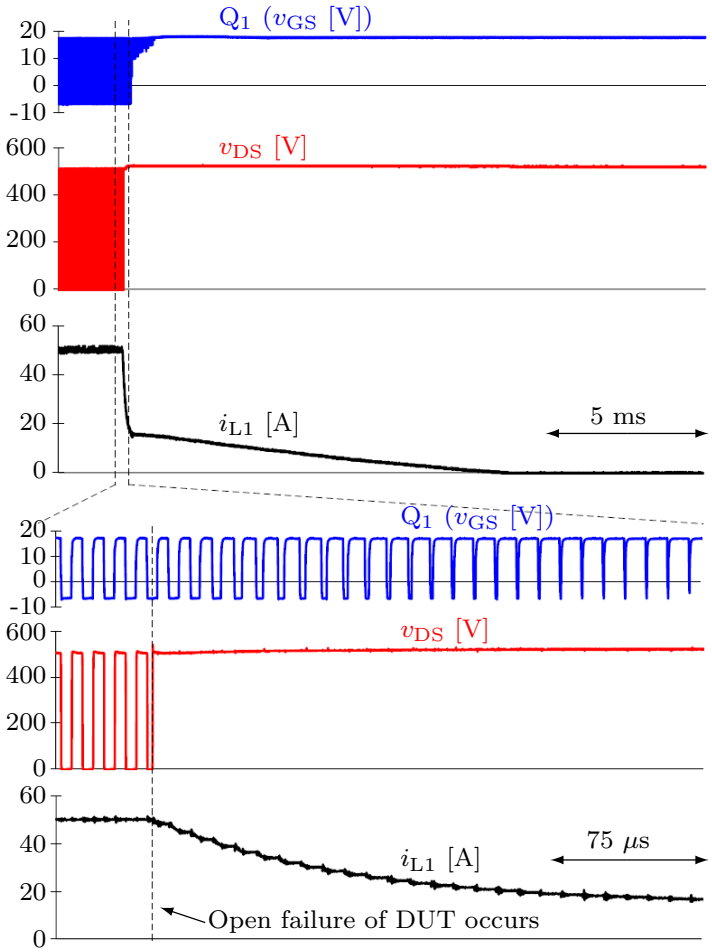


Fig.3.28. Experimental gate waveform and inductor current waveform when open failure of the DUT occurs.

Fig. 3.28 shows the experiment waveforms when open failure of the DUT occurs. After the open failure, and when the transistor Q_1 is on, the inductor current i_{L1} is freewheeling in the circuit. Therefore, the reduction rate of the inductor current i_{L1} is small. In contrast, when transistor Q_1 is off, the inductor current i_{L1} charges the capacitor C_1. Therefore, the reduction rate of the inductor current i_{L1} is large. Whether the transistor Q_1 is on or off, the inductor current i_{L1} gradually reaches 0 A. The drain-source voltage of the DUT was equal to the capacitor voltage v_{C1}; thus, the maximum value of the capacitor voltage V_{Cmax} was applied to the drain-source of the DUT. The maximum value of the DUT drain-source voltage was 522 V, 4.4% higher than the test voltage V_{DS} = 500 V. Furthermore, the maximum value was approximately equal to the value (523 V) calculated using Eq. 3.7. The

Table.3.8 Experimental conditions of the boost-type test circuit.

Contents	Value
Test voltage V_{DS}	800 V
Test current I_D	20 A
Switching frequency f_{SW}	100 kHz
Duty ratio of DUT D_D	0.5
Overcurrent detection value I_{OC}	30 A

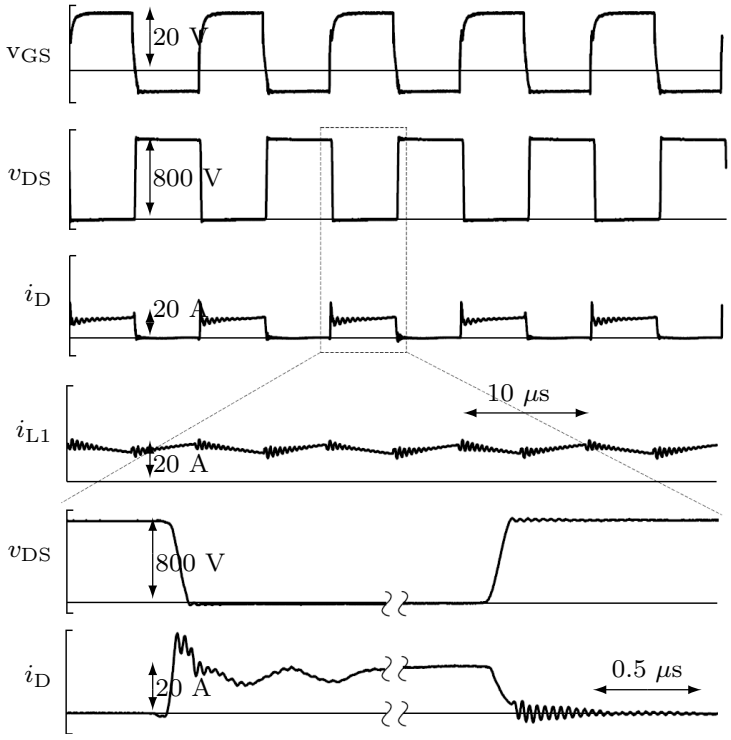


Fig.3.29. Experimental waveforms of the boost-type test circuit.

test circuit can be stopped without spreading the failure to the test circuit.

3.5.2 Boost-type Test Circuit

Tab. 3.8 depicts the experimental conditions of the boost-type test circuit. The test voltage V_{DS} was set to 800 V, larger than the rated voltage of the DC power supply. The test current I_D was set to 20 A. Under these conditions, the conversion capacity was 8 kW because the duty ratio of the DUT was set to 0.5.

Fig. 3.29 depicts the experiment waveforms during normal operation. The test current I_D was measured by the Rogowski coil; hence, the DC component is offset in Fig. 3.29. The current ripple ΔI_D was 5.6 A, which is in good agreement with

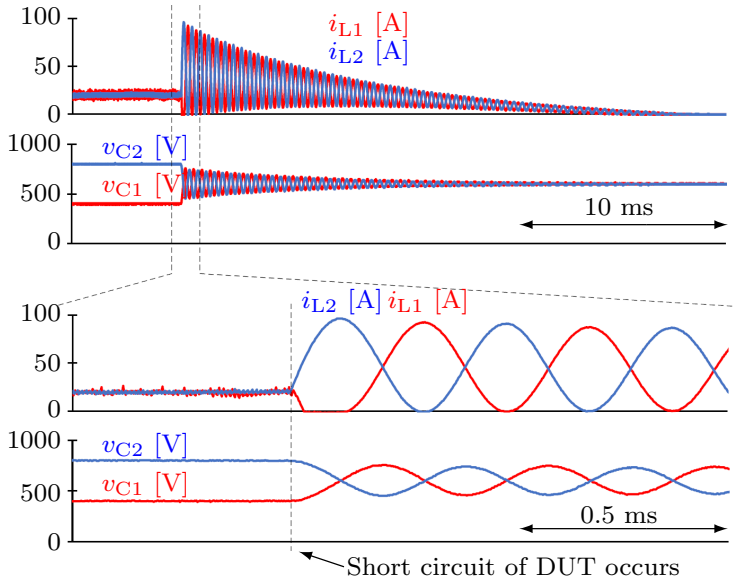


Fig.3.30. Experimental waveforms when short circuit failure of the DUT occurs.

the calculated value obtained by applying Eq. 3.23. The input power of the DC power supply was 480 W, which was 6.1% of the conversion capacity.

Fig. 3.30 shows the experimental waveforms when a short circuit of the DUT occurs. At this time, the overcurrent set value of the inductor current i_{L2} was set to 30 A. The transistor Q_1 stopped operating owing to the detection of an overcurrent. The maximum current I_{Lmax} was 97 A, 8% smaller than the value calculated using Eq. 3.19. The reason for the error is that the approximate expressions were applied to Eq. 3.19, and the resistance components in the circuit were not considered in the worst case. The inductor currents i_{L1} and i_{L2} gradually decreased and reached 0 A. The maximum voltage V_{Cmax} did not exceed the test voltage V_{DS}, and the capacitor voltages v_{C1} and v_{C2} converged to an intermediate value between the input voltage E and test voltage V_{DS}. Therefore, the test can be stopped without spreading the DUT failure to the test circuit.

Fig. 3.31 shows the experiment waveforms when open failure of the DUT occurs. After open failure of the DUT, the inductor current i_{L2} decreased. At this time, a low inductor current i_{L2} was detected, and the operation of the transistor Q_1 was stopped (the low current detection value was set to 5 A in this experiment).

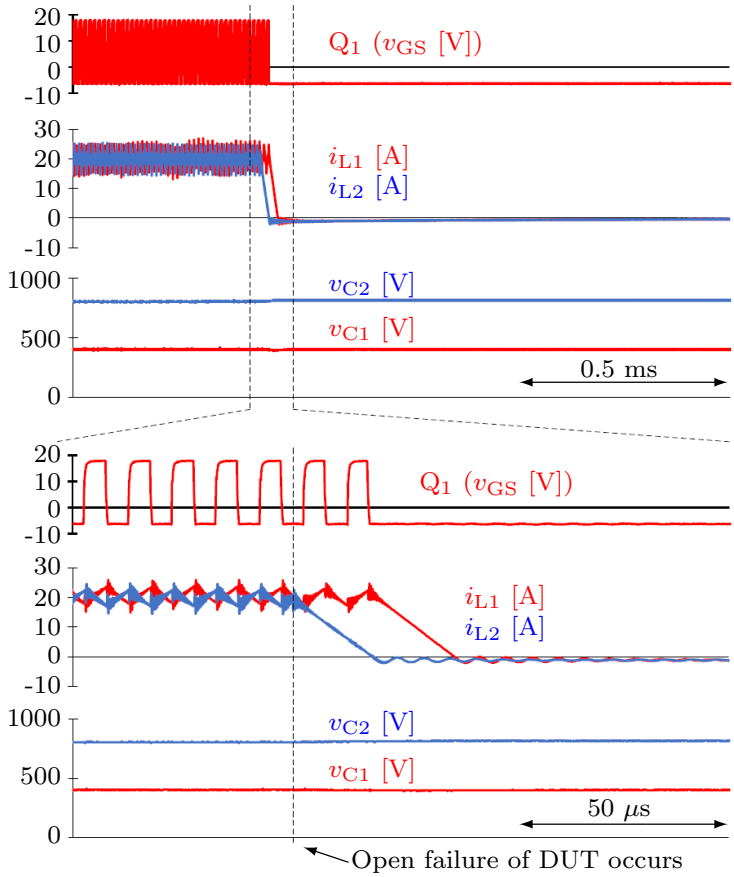


Fig.3.31. Experimental waveforms when open failure of the DUT occurs.

Subsequently, the inductor current i_{L1} decreased. The maximum voltage V_{Cmax} was smaller than the value calculated by Eq. 3.20 because the operation of the transistor Q_1 could be stopped by detecting the low inductor current i_{L2}.

3.6 Development of Gate Drive Circuit for DUT

Fig. 3.32 shows the advanced HTGB test circuit. The continuous switching circuit includes the cascaded buck-boost converter. The gate drive circuit for the DUT was specifically designed to output an overvoltage attributable to the accelerated aging for gate oxide. The gate drive circuit consisted of a half-bridge inverter. The test gate–source voltages, V_{Gp} and V_{Gn}, could be set using the DC power supplies, and the following design was used to prevent the failure from spreading to the gate driver circuit (in case the DUT failed during the accelerated

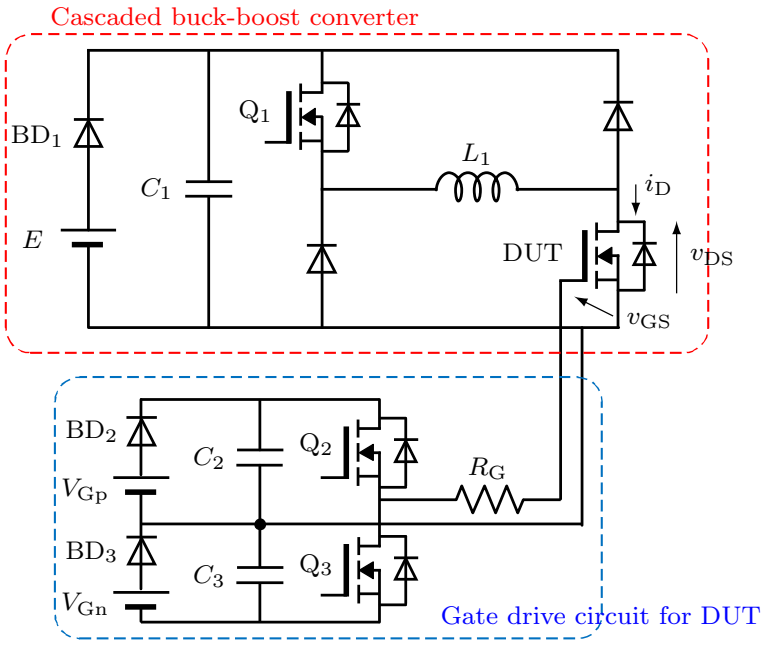


Fig.3.32. Advanced HTGB test circuit.

aging test):

- Switching elements Q_2 and Q_3 had the same rated voltage as switching element Q_1 in the continuous switching circuit.
- Capacitors C_2 and C_3 had the same rated voltage as capacitor C_1 in the continuous switching circuit.
- Blocking diodes BD_2 and BD_3 had the same rated voltage as blocking diode BD_1 in the continuous switching circuit, to prevent overvoltage from being applied to the DC power supplies.

Fig. 3.33 shows the fabricated gate drive circuit for the DUT. Fig. 3.34 shows its experimental waveform. The experimental conditions were as follows: $V_{Gp} = 50$ V, $V_{Gn} = 0$ V, switching frequency $f_{SW} = 100$ kHz, and on-duty ratio $D_D = 0.5$. The output of the gate drive circuit was open (no-load). From Fig. 3.34, it can be confirmed that the voltage waveform was outputted according to the specifications.

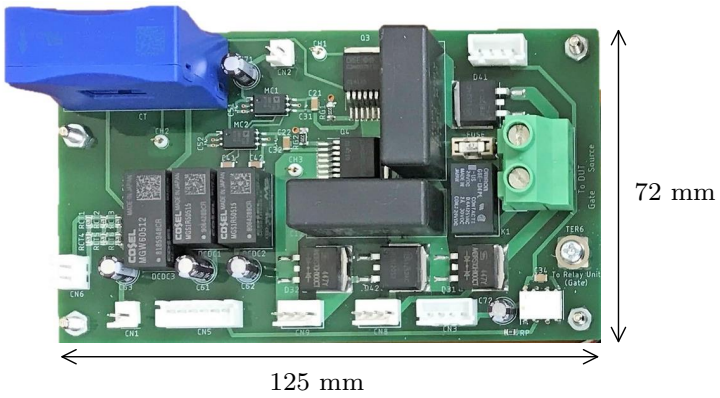


Fig.3.33. Fabricated gate drive circuit for DUT.

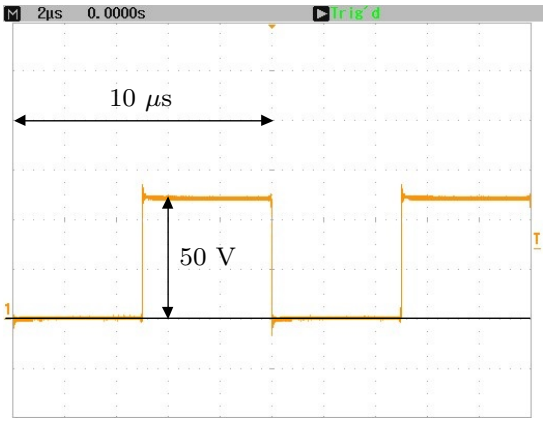


Fig.3.34. Experimental waveforms of the gate drive circuit for DUT.

3.7 Summary

An accelerated aging method and its test circuit were developed to verify the degradation characteristics of SiC MOSFETs implemented in power conversion circuits.

An advanced HTGB test method combining conventional HTGB testing and continuous switching tests was proposed. The advanced HTGB test circuit was divided into a continuous switching circuit and a gate drive circuit for the DUT.

In the development of the continuous switching circuit, two types of test circuits (and their design method) were proposed. Compared with the boost-type test circuit, the buck-type test circuit offers the following advantages: the DUT acts as a low-side transistor, which is suitable for measurement; the number of components

is small; and the circuit design easily accounts for abnormal operation. On the other hand, when a test voltage exceeding the output voltage of the existing DC power supply is required, the boost-type test circuit is suitable. Furthermore, the proposed test circuits do not implement complicated protection circuits, thereby facilitating a simplified test circuit configuration. This facilitates the preparation of multiple test circuits to simultaneously test numerous samples. The proposed design method was verified using a circuit simulation, and the circuit operation was verified using an experimental circuit under conditions of 500 V, 50 A and 800 V, 20 A; the effectiveness of the design method was demonstrated.

In the development of a gate drive circuit for the DUT, a circuit was developed to output a voltage exceeding the rated gate–source voltage (caused by the accelerated aging of the gate oxide) of the DUT.

Chapter 4

Characteristic Fluctuations of SiC MOSFETs Due to Oxide Charge

This chapter presents an experimental verification of the theoretical study in Section 2.2, to show that the C_{iss}–v_{GS} characteristic is suitable as an aging precursor for condition monitoring.

Through accelerated aging tests for the gate oxide of SiC MOSFETs under switching conditions, the C_{iss}–v_{GS} characteristic is verified to fluctuate under gate oxide degradation. First, the degradation of the gate oxide is verified using the conventional accelerated aging method as well as the advanced HTGB test method (to verify the degradation characteristics of different test methods). Next, four types of commercially available 1.2 kV SiC MOSFETs are used as DUTs for the accelerated aging test, to verify the degradation characteristics of different types of DUTs. Finally, characteristic fluctuations of C_{iss}–v_{GS} caused by degradation or temperature dependence are discussed based on the experimental results.

4.1 Comparison of Conventional and Advanced HTGB Test Results

4.1.1 Test Conditions

In this section, HTGB tests were performed on one type of SiC MOSFET DUT under various conditions. The purpose of performing HTGB tests under various conditions was to verify the test-condition-dependent differences in test results.

Commercially available SiC MOSFETs were used as DUTs. Tab. 4.1 presents the specifications of the DUT [114].

Table.4.1 Specifications of the DUT [114].

Parameters	Value
Manufacturer	Cree
Model name	C2M0280120D
Gate structure	Planar type
Rated drain–source voltage	1200 V
Rated drain current	11 A
Rated gate–source voltage	+25/−10 V
Maximum junction temperature	150 °C

Table.4.2 Test conditions for various HTGB tests.

No.	Test type	$V_{\mathrm{Gp}}/V_{\mathrm{Gn}}$	V_{DS}	I_{D}	f_{SW}	Temperature
i)	Conventional	44/− V	0 V	0 A	–	$T_{\mathrm{c}} = 150°\mathrm{C}$
ii)	Advanced	44/0 V	300 V	2 A	100 kHz	$T_{\mathrm{c}} = 140°\mathrm{C}$
iii)	Advanced	44/0 V	500 V	5 A	100 kHz	Implemented on heat sink

The test conditions are shown in Tab. 4.2. Test condition i) was the conventional HTGB test method. The test circuit is shown in Fig. 3.1(a). The test gate voltage was DC and set to 44 V. The test voltage V_{DS} was 0 V (short). The DUT experiment was implemented on a hot plate to achieve a case temperature of $T_{\mathrm{c}} = 150°\mathrm{C}$. That is, the junction temperature of the DUT was estimated to be 150°C, matching the case temperature.

Test condition ii) represented the advanced HTGB test method. The positive test gate voltage was set to $V_{\mathrm{Gp}} = 44$ V, as in test condition i). The negative test gate voltage V_{Gn} was set to 0 V, to verify the degradation tendency when the gate–source voltage was positive; the reason for this is that SiC MOSFETs in power conversion circuits are often used with $V_{\mathrm{Gn}} = 0$ V. The test voltage was set to $V_{\mathrm{DS}} = 300$ V, the test current was set to $I_{\mathrm{D}} = 2$ A, the switching frequency was set to $f_{\mathrm{SW}} = 100$ kHz, and the on-duty ratio was set to $D_{\mathrm{D}} = 0.5$. To make the estimated junction temperature of the DUT equal to that of test condition i), the DUT was implemented on a hot plate to achieve the case temperature $T_{\mathrm{c}} = 140°\mathrm{C}$. The reason for setting the case temperature at $T_{\mathrm{c}} = 140°\mathrm{C}$ is that the junction temperature during the test is estimated to be 150°C, according to the generated loss and thermal resistance of the DUT, as verified beforehand.

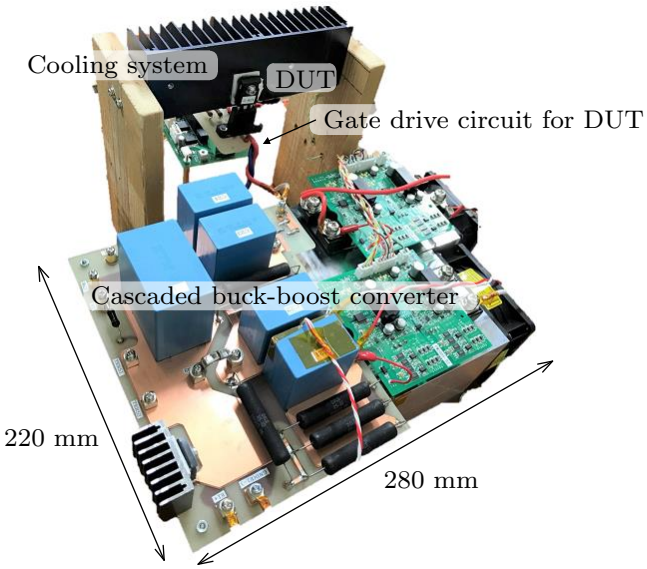


Fig.4.1. Experimental setup for the advanced HTGB test.

Test condition iii) was set in consideration of the actual operating conditions of the DUT. The positive test gate voltage was set to $V_{\mathrm{Gp}} = 44$ V and the negative test gate voltage V_{Gn} was set to 0 V as in test conditions i) and ii). The test voltage was set to $V_{\mathrm{DS}} = 500$ V, the test current was set to $I_{\mathrm{D}} = 5$ A, the switching frequency was set to $f_{\mathrm{SW}} = 100$ kHz, and the on-duty ratio was set to $D_{\mathrm{D}} = 0.5$. The DUT experiment was implemented on a heatsink for cooling. The thermal resistance of the cooling system (including heatsink) was 7 K/W. The ambient temperature during the test was 25 °C. In test conditions iii), the junction temperature of the DUT was uncontrolled. Therefore, the junction temperature increased as the loss increased or decreased, owing to the degradation of the DUT. This situation resembled that of the power devices used in actual power conversion circuits. However, the junction temperature of the DUTs did not exceed the maximum value given in the datasheet (150°C) during the test involving the cooling system.

For test conditions ii) and iii), the advanced HTGB test circuit shown in Fig. 3.32 was used. Fig. 4.1 shows the experimental setup for test condition iii).

Three samples were tested under each of the test conditions i) to iii). Dur-

TABLE.4.3 MEASURED ELECTRICAL CHARACTERISTICS AND MEASUREMENT CONDITIONS.

Symbols	Parameters	Measurement conditions
V_{th}	Gate threshold voltage	$v_{\mathrm{DS}} = v_{\mathrm{GS}}$, $i_{\mathrm{D}} = 1.25$ mA
$R_{\mathrm{DS(ON)}}$	On-resistance	$v_{\mathrm{GS}} = 20$ V, $i_{\mathrm{D}} = 6$ A
–	C_{iss}–v_{GS} characteristics	$v_{\mathrm{DS}} = 0$ V, $v_{\mathrm{AC}} = 25$ mV (1 MHz)

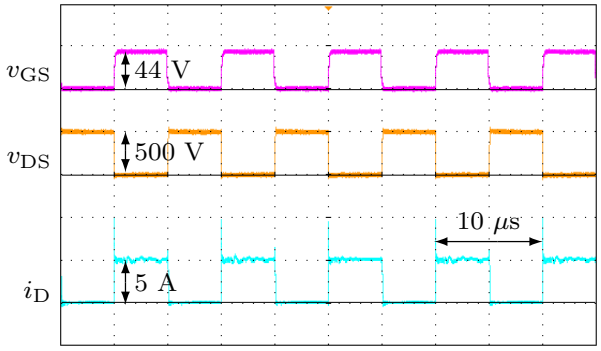


Fig.4.2. Experimental waveforms of test condition iii).

ing the test, the electrical characteristics were measured at certain intervals at room temperature (25°C). The measured parameters were the gate threshold voltage V_{th}, on-resistance $R_{\mathrm{DS(ON)}}$, and input capacitance C_{iss}–v_{GS} characteristics. The measurement conditions are shown in Tab. 4.3. These characteristics were measured using a semiconductor curve tracer (CS-3200, Iwatsu) and high-voltage capacitance–voltage (C–V) measurement system (CS-603A, Iwatsu). All tests were performed until the DUT failed. In those tests, all DUTs registered short-circuit failures, and the continuous switching circuit stopped the operation.

4.1.2 Test Results and Discussion

Fig. 4.2 shows the experimental waveforms of test condition iii). The experimental waveforms conformed to the test conditions. Fig. 4.3 shows the fluctuation of the gate threshold voltage V_{th}. Test condition i) had the shortest average time to DUT failure, followed by iii) and finally ii). In test conditions i) and ii), the gate threshold voltage V_{th} tended to decrease in the initial stage. Later, the gate threshold voltage V_{th} increased and led to DUT failure. On the other hand, in test condition iii), the gate threshold voltage V_{TH} decreased, leading directly to DUT

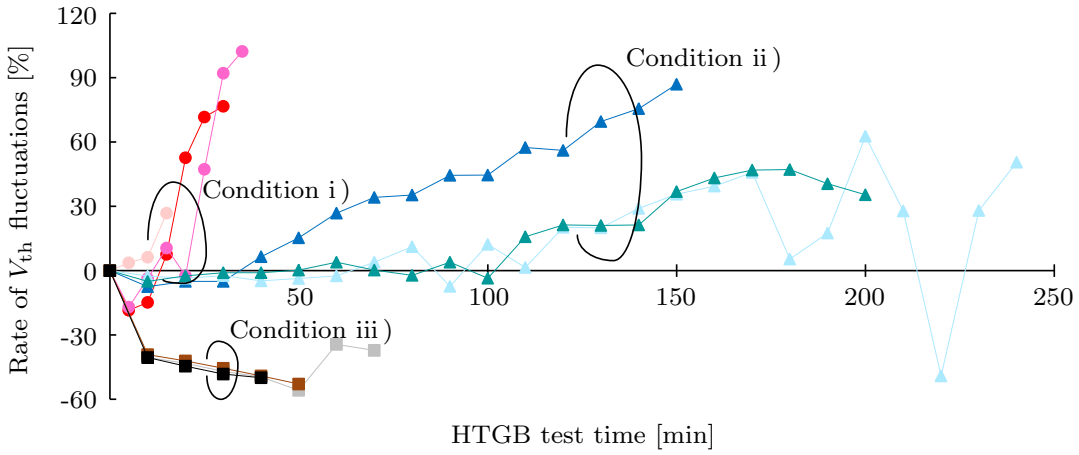


Fig.4.3. HTGB test results under various conditions (fluctuations of gate threshold voltage V_{th}).

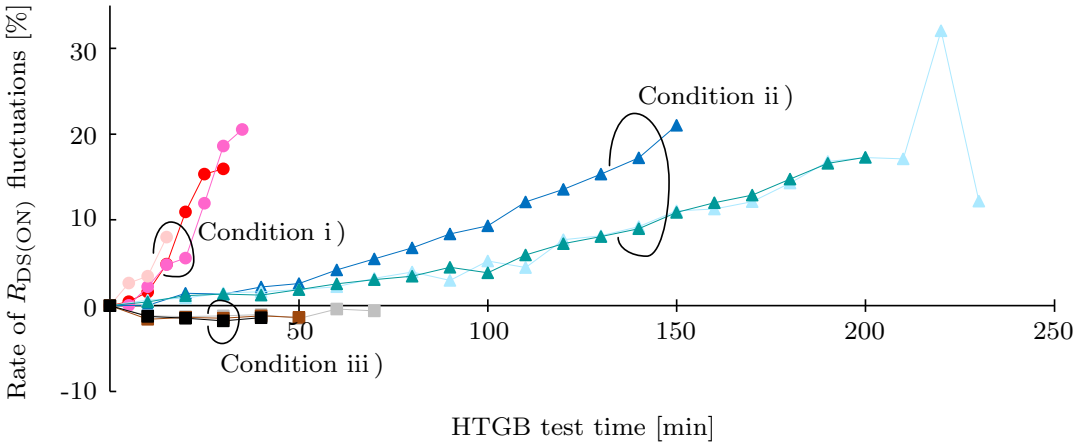


Fig.4.4. HTGB test results under various conditions (fluctuations of on-resistance $R_{\mathrm{DS(ON)}}$).

failure.

Fig. 4.4 shows the fluctuation of the on-resistance $R_{\mathrm{DS(ON)}}$. In test conditions i) and ii), the on-resistance increased, leading directly to DUT failure. On the other hand, in test condition iii), the on-resistance $R_{\mathrm{DS(ON)}}$ remained almost the same or decreased slightly, leading to DUT failure.

Figs. 4.5–4.7 show the fluctuation of the input capacitance C_{iss} versus the gate–source voltage v_{GS} characteristic (C_{iss}–v_{GS} characteristic) under test conditions i)–iii), respectively. No significant difference was observed between samples under different test conditions; hence, only the C_{iss}–v_{GS} characteristics of one sample are

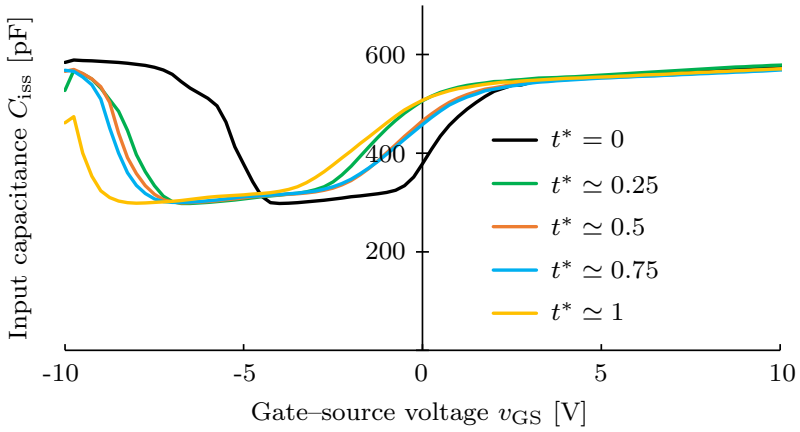


Fig.4.5. Fluctuation of C_{iss}–v_{GS} characteristics under test condition i).

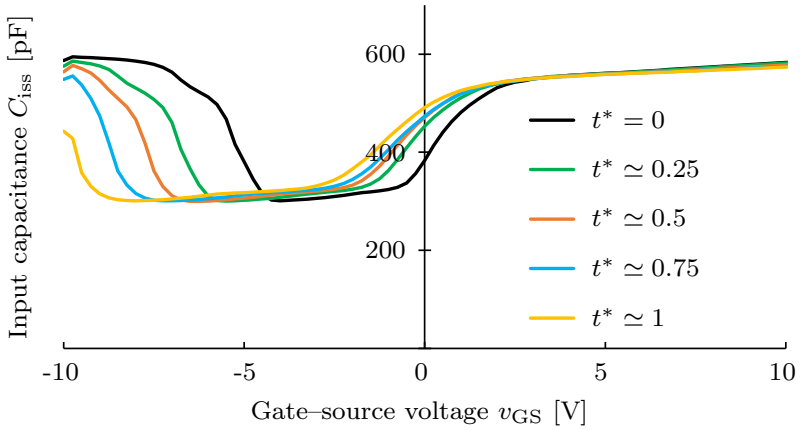


Fig.4.6. Fluctuation of C_{iss}–v_{GS} characteristics under test condition ii).

shown. Here, the standardized stress-applied time t^* is defined as

$$t^* = t/t_{\mathrm{BD}}, \tag{4.1}$$

where t is the HTGB test time and t_{BD} is the DUT failure time. The C_{iss}–v_{GS} characteristic fluctuated under the degradation of the gate oxide (details are presented in Section 2.2). Therefore, the fluctuations of gate threshold voltage V_{th} and on-resistance $R_{\mathrm{DS(ON)}}$ were considered to be produced by the degradation of the gate oxide.

From the experimental results, it was clarified that the degradation trend differed according to the HTGB test conditions. Because this dissertation does not aim to analyze the detailed degradation mechanisms of SiC MOSFETs, the differences in the degradation trends attributable to different test conditions are not

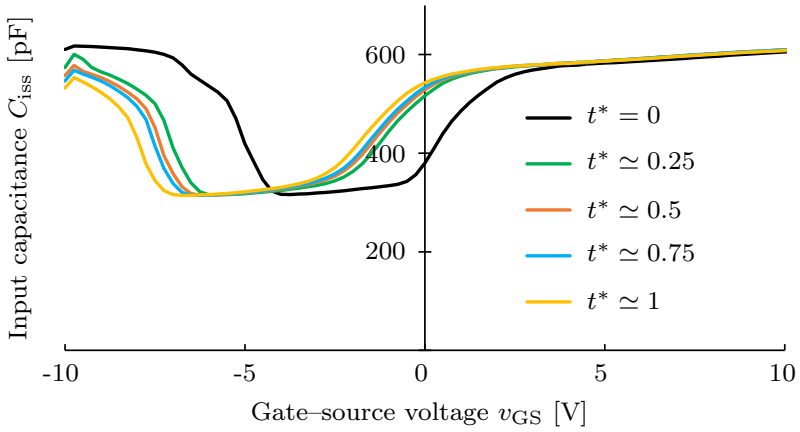


Fig.4.7. Fluctuation of C_{iss}–v_{GS} characteristics under test condition iii).

discussed in detail. However, it remains desirable to perform accelerated aging tests of power devices for condition monitoring, taking into account the voltage, current, and switching frequency at which devices are operated.

4.2 Comparison of Advanced HTGB Test Results for Four Types of SiC MOSFETs

4.2.1 Test Conditions

In this section, HTGB tests are performed on four types of SiC MOSFET DUTs under one condition. The purpose of performing HTGB tests for four types of SiC MOSFETs is to verify the differences in test results with respect to the type of DUT.

Tab. 4.4 shows the specifications of the selected SiC MOSFETs, which are all commercially available 1.2 kV SiC MOSFETs of the discrete type [114]–[117]. Planar-type and trench-type gate structures were considered.

Table.4.4 Specifications of DUTs [114]–[117].

Name of DUT	DUT–A	DUT–B	DUT–C	DUT–D
Manufacturer	Cree	ROHM	ROHM	Infineon
Model name	C2M0280120D	SCT2280KE	SCT3160KL	IMW120R220M1H
Gate structure	Planar	Planar	Trench	Trench
Rated drain–source voltage	1200 V	1200 V	1200 V	1200 V
Rated drain current	11 A	14 A	17 A	13 A
Rated gate–source voltage	+25/−10 V	+26/−10 V	+26/−4 V	+23/−7 V
Maximum junction temperature	150 °C	175 °C	175 °C	175 °C

Table.4.5 Test condition of HTGB tests for four types of SiC MOSFETs.

Test type	V_{Gp}/V_{Gn}	V_{DS}	I_D	f_{SW}	Temperature
Advanced	Refer to Tab. 4.6	500 V	5 A	100 kHz	Implemented on heat sink

Table.4.6 Test gate–source voltage V_{Gp} and V_{Gn}

Name of DUT	DUT–A	DUT–B	DUT–C	DUT–D
V_{BD}	49 V	48 V	59 V	76.5 V
V_{Gp} (90% of V_{BD})	44 V	43 V	53 V	69 V
V_{Gn}	0 V	0 V	0 V	0 V

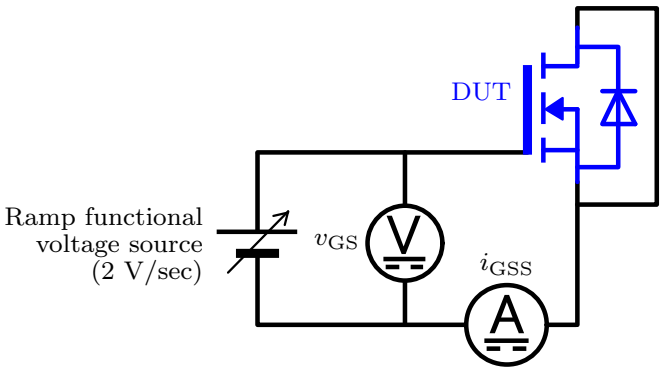


Fig.4.8. TZDB test circuit diagram.

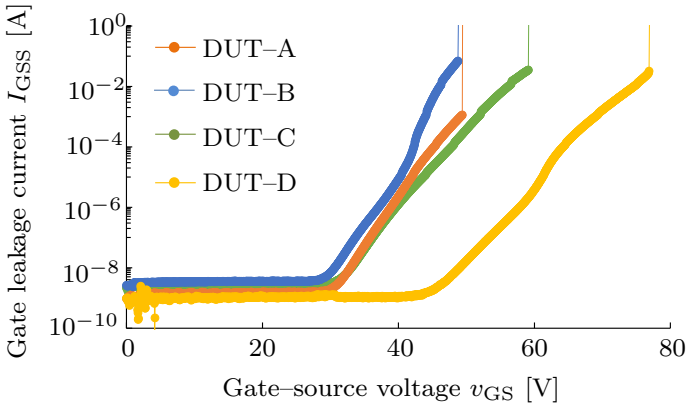


Fig.4.9. TZDB test results for the four types of SiC MOSFETs.

To determine the test gate voltage V_{Gp} for the advanced HTGB test, the gate oxide time zero dielectric breakdown (TZDB) voltages V_{BD} of the four types of SiC MOSFETs were measured. The purpose of the TZDB test was to determine the test gate voltage V_{Gp} for the advanced HTBG, rather than to evaluate the exact TZDB voltage. Therefore, the number of samples for each DUT was one. Fig. 4.8 shows the test circuit diagram for the TZDB test. In the TZBD test, the ramp functional voltage (2 V/sec) outputted from a ramp functional voltage source was applied between the gate and source of the DUT, and the gate leakage current i_{GSS} was measured using a DC ammeter (DMM6500, Tektronix). Fig. 4.9 shows the TZDB test results for the four types of SiC MOSFETs. The highest dielectric breakdown voltage (V_{BD} of DUT–D) was 1.5 times that of the lowest (V_{BD} of DUT–B). Moreover, in this case, the V_{BD} of the DUT with the trench-type gate structure tended to exceed that of the planar-type DUT.

Table.4.7 Measured electrical characteristics and measurement conditions.

Symbols	Parameters	Measurement conditions
V_{th}	Gate threshold voltage	$v_{\mathrm{DS}} = v_{\mathrm{GS}}$, $i_{\mathrm{D}} = 1.25$ mA
$R_{\mathrm{DS(ON)}}$	On-resistance	$v_{\mathrm{GS}} = 20$ V, $i_{\mathrm{D}} = 6$ A
–	C_{iss}–v_{GS} characteristic	$v_{\mathrm{DS}} = 0$ V, $v_{\mathrm{AC}} = 25$ mV (1 MHz)
–	i_{D}–v_{GS} characteristic	$v_{\mathrm{DS}} = 20$ V

The HTGB test conditions are shown in Tabs. 4.5 and 4.6. The positive test gate voltage V_{Gp} was set to 90% of the TZDB voltage V_{BD}, as shown in Fig. 4.9. The other test conditions were the same as for test condition iii), as described in Section 4.1. The negative test gate voltage was set to $V_{\mathrm{Gn}} = 0$ V, the test voltage was set to $V_{\mathrm{DS}} = 500$ V, the test current was set to $I_{\mathrm{D}} = 5$ A, the switching frequency was set to $f_{\mathrm{SW}} = 100$ kHz, and the on-duty ratio was set to $D_{\mathrm{D}} = 0.5$. The case of the DUT was implemented on a heatsink for cooling. The thermal resistance of the cooling system (including heatsink) was 7 K/W. The ambient temperature during the test was 20 °C and the junction temperature was set not to exceed the maximum rating.

Three samples were tested for each of the four types of SiC MOSFETs: DUT–A to DUT–D. During the test, the electrical characteristics were measured at certain intervals at room temperature (20°C). The measured parameters were the gate threshold voltage V_{TH}, on-resistance $R_{\mathrm{DS(ON)}}$, C_{iss}–v_{GS} characteristic, and drain current i_{D} with respect to gate–source voltage v_{GS} characteristic (i_{D}–v_{GS} characteristics). The measurement conditions are shown in Tab. 4.7. The duration of the test was set to 300 min, to detect degradation according to fixed test conditions. However, when the DUT suffered a failure or the static characteristics of the DUT became unmeasurable before 300 min, the test was stopped.

4.2.2 Test Results and Discussion

Figs. 4.10 and 4.11 show the results of the advanced HTGB test (degradation characteristics) in DUT–A. The DUT failures occurred in all three samples within 80 min. Figs. 4.10 and 4.11 show that the gate threshold voltage V_{th} and on-

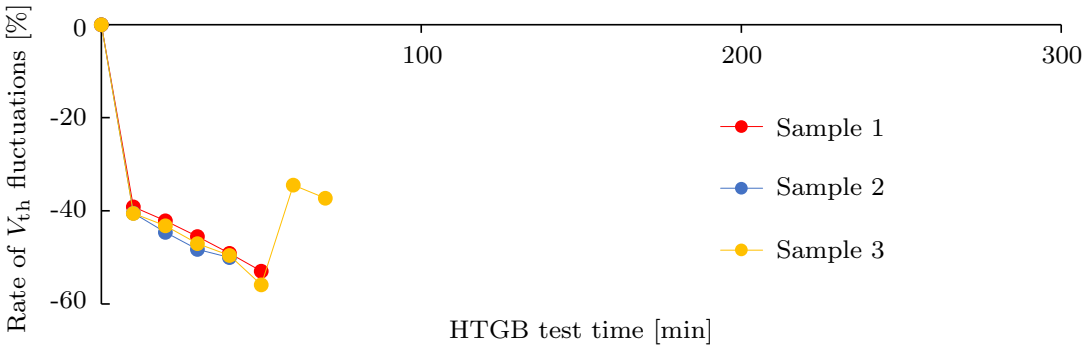


Fig.4.10. HTGB test results for DUT–A (fluctuations of gate threshold voltage V_{th}).

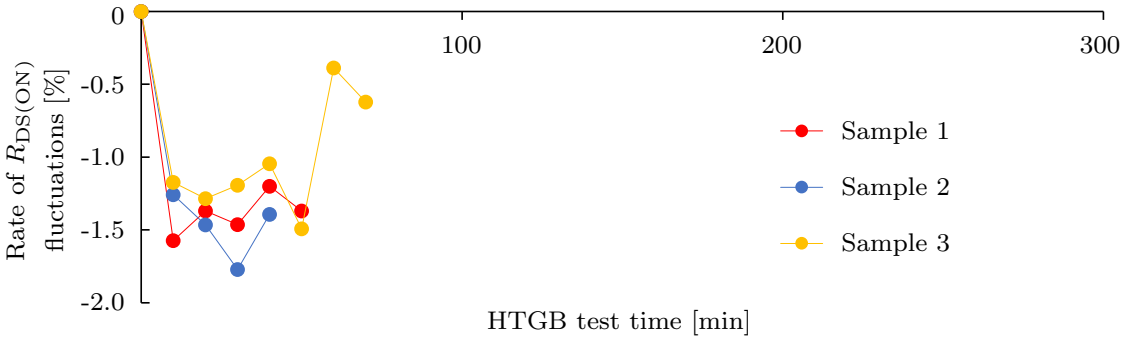


Fig.4.11. HTGB test results for DUT–A (fluctuations of gate threshold voltage $R_{\mathrm{DS(ON)}}$).

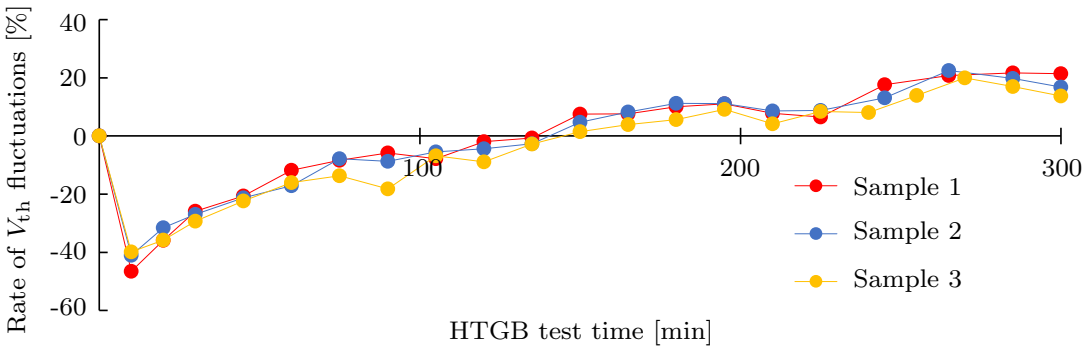


Fig.4.12. HTGB test results for DUT–B (fluctuations of gate threshold voltage V_{th}).

resistance $R_{\mathrm{DS(ON)}}$ tended to decrease compared to the initial values, which eventually led to DUT failure. The on-resistance $R_{\mathrm{DS(ON)}}$ was within the datasheet's guaranteed value; however, the threshold voltage V_{th} was below this value. The decrease in the threshold voltage can be attributed to the migration of the mobile oxide charge in the gate oxide to the vicinity of the oxide–semiconductor interface.

Figs. 4.12 and 4.13 show the results of the advanced HTGB test (degradation

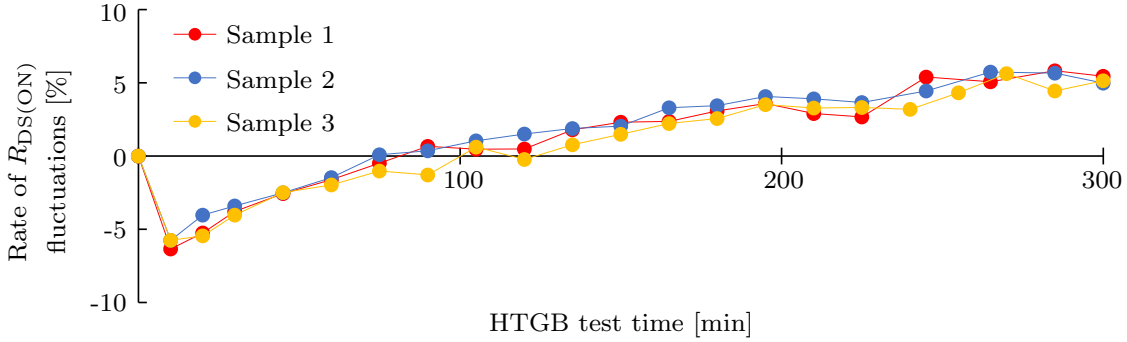


Fig.4.13. HTGB test results for DUT–B (fluctuations of gate threshold voltage $R_{DS(ON)}$).

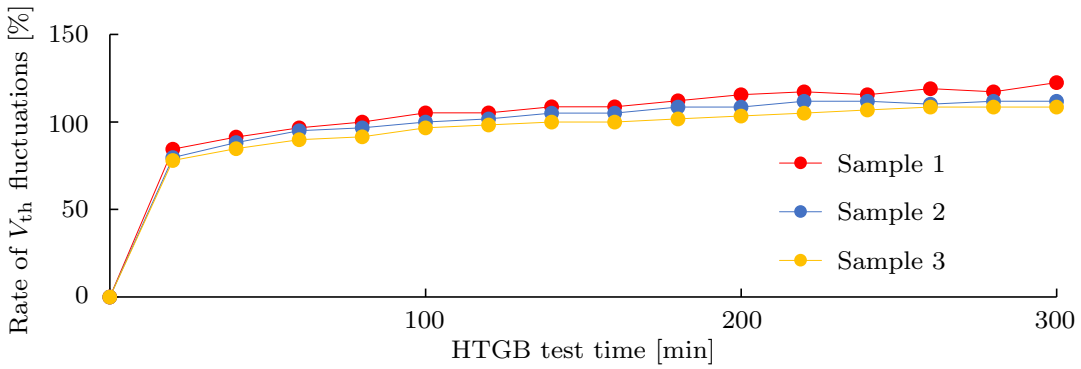


Fig.4.14. HTGB test results for DUT–C (fluctuations of gate threshold voltage V_{th}).

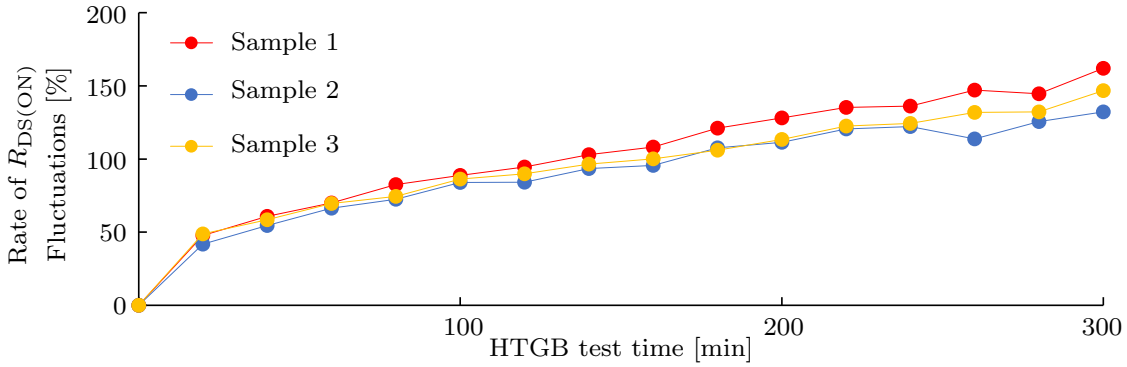


Fig.4.15. HTGB test results for DUT–C (fluctuations of gate threshold voltage $R_{DS(ON)}$).

characteristics) for DUT–B. One of the DUTs failed immediately after the test began, owing to the gate oxide dielectric breakdown. Therefore, the other sample was added as the DUT. For these three DUTs, the DUTs did not fail, even after 300 min. From Figs. 4.12 and 4.13, the gate threshold voltage V_{th} and on-resistance $R_{DS(ON)}$ tended to first decrease and then increase compared to the initial values. The on-resistance $R_{DS(ON)}$ was within the datasheet's guaranteed value; however, the threshold voltage V_{TH} varied and almost exceeded this value.

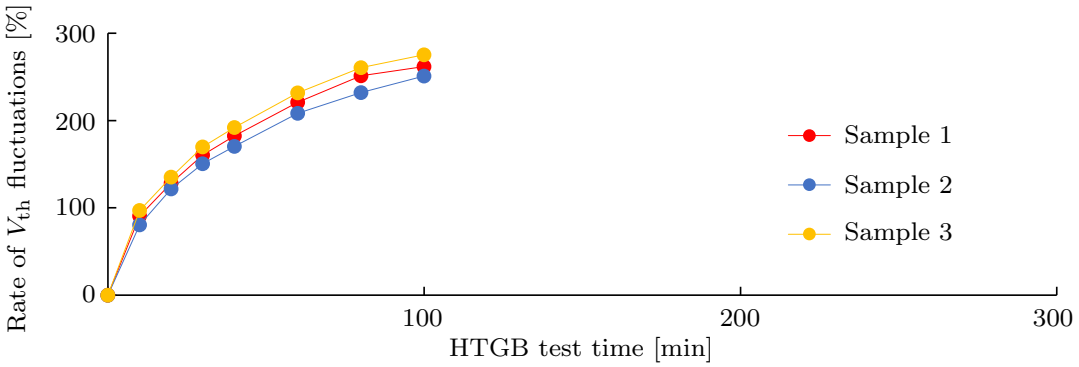


Fig.4.16. HTGB test results for DUT–D (fluctuations of gate threshold voltage V_{th}).

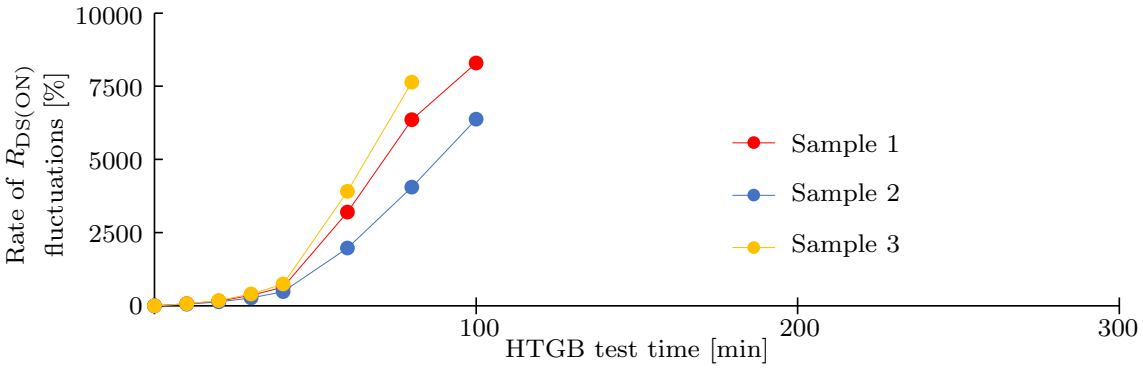


Fig.4.17. HTGB test results for DUT–D (fluctuations of gate threshold voltage $R_{\mathrm{DS(ON)}}$).

Figs. 4.14 and 4.15 show the results of the advanced HTGB test (degradation characteristics) for DUT–C. Similar to DUT–B, the DUTs did not fail after 300 min. Figs. 4.14 and 4.15 show that the gate threshold voltage V_{th} and on-resistance $R_{\mathrm{DS(ON)}}$ tended to increase compared to the initial values, fluctuating to a value above the maximum guaranteed one.

Figs. 4.16 and 4.17 show the results of the advanced HTGB test (degradation characteristics) for DUT–D. It was not possible to determine when the DUTs would fail because the test was stopped after 100 min owing to the on-resistance $R_{\mathrm{DS(ON)}}$, which became immeasurably large. The on-resistance $R_{\mathrm{DS(ON)}}$ increased exponentially within the test time. The gate threshold voltage V_{th} tended to increase beyond the initial value and fluctuated to a value exceeding the maximum guaranteed one.

As shown in Figs. 4.14 and 4.17, the DUT with the trench-type gate structure

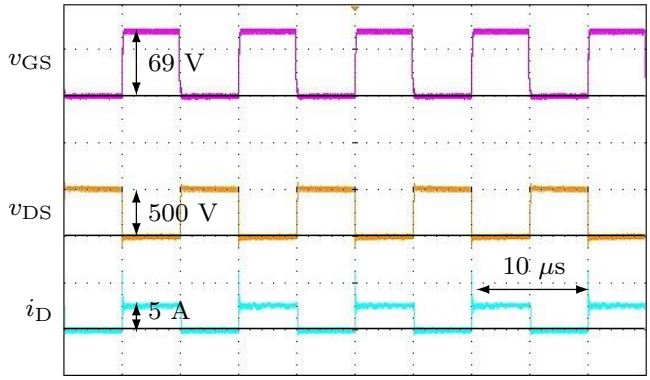


Fig.4.18. Advanced HTGB test waveforms for DUT–D (Sample 1) at 0 min.

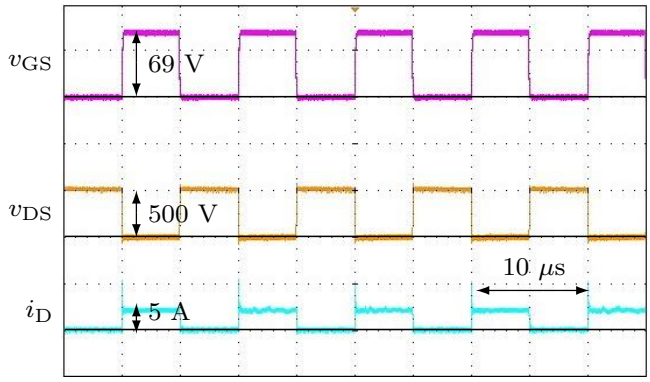


Fig.4.19. Advanced HTGB test waveform for DUT–D (Sample 1) at 300 min.

showed a significant fluctuation in both the gate threshold voltage V_{th} and on-resistance $R_{\text{DS(ON)}}$, when compared to the datasheet's guaranteed value. Figs. 4.18 and 4.19 show the advanced HTGB test waveforms of DUT–D (sample 1) at 0 min and 300 min, respectively. The experimental waveforms conformed to the test conditions. Moreover, despite the drastic change in the static characteristics, no significant change was observed in the switching waveform.

Different trends in the degradation characteristics were observed for the four types of DUTs. In contrast, three samples showed the same degradation characteristic trends for the same type of DUT. Thus, different manufacturers and gate structures may lead to different processes and integrations and therefore different devices. The same result was obtained for different samples of the same DUT. This result suggests that the process is under control.

The fluctuation of the gate threshold voltage V_{th} and on-resistance $R_{\text{DS(ON)}}$ is

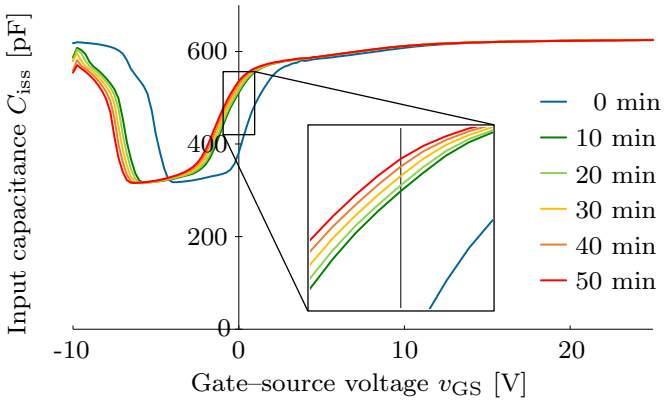


Fig.4.20. C_{iss}–v_{GS} characteristics for DUT–A.

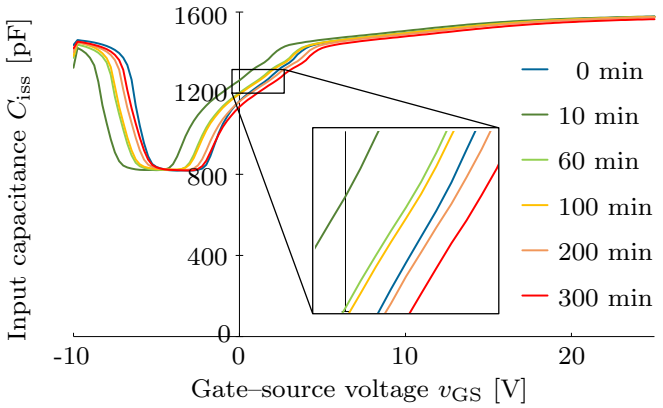


Fig.4.21. C_{iss}–v_{GS} characteristics for DUT–B

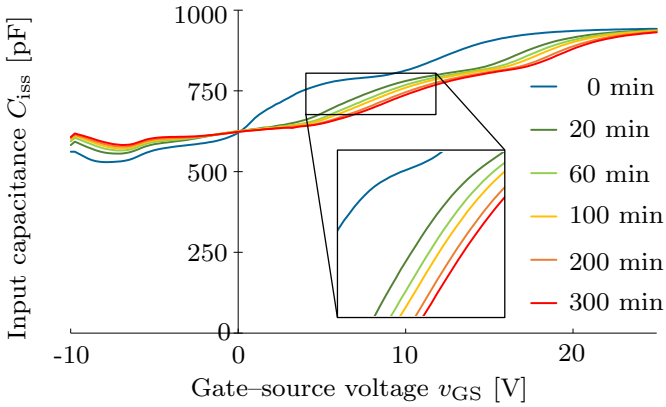


Fig.4.22. C_{iss}–v_{GS} characteristics for DUT–C.

discussed according to the input capacitance C_{iss}–v_{GS} characteristics [118]. Figs. 4.20–4.23 show the C_{iss}–v_{GS} characteristics of DUT–A, DUT–B, DUT–C, and DUT–D, respectively. The C_{iss}–v_{GS} characteristics were measured for sample 1, as shown in Figs. 4.10 to 4.17 for each DUT. The C_{iss}–v_{GS} characteristics were

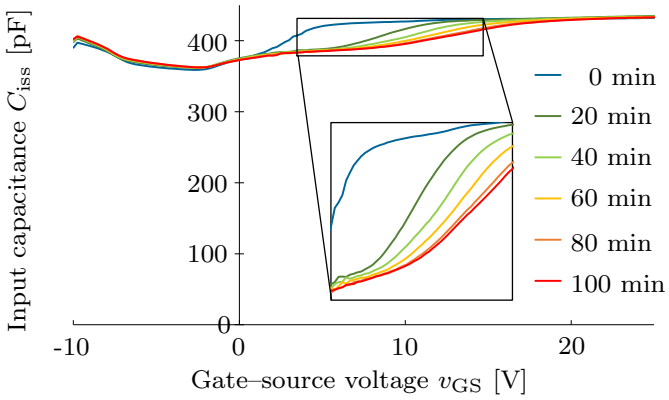


Fig.4.23. C_{iss}–v_{GS} characteristics for DUT–D

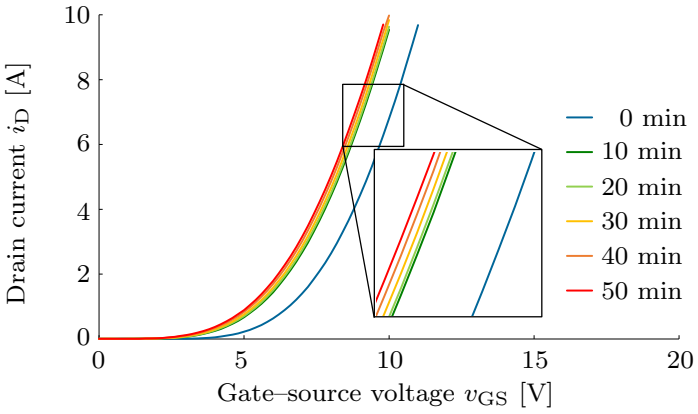


Fig.4.24. i_D–v_{GS} characteristics for DUT–A.

measured using a high-frequency C–V method, to evaluate trapped charges in the oxide or oxide–semiconductor interface.

The fluctuation of the threshold voltage V_{th} was considered to be caused by the mobile oxide charge and oxide-trapped charge in the gate oxide above the channel region. In Figs. 4.20–4.23, the enlarged areas are those where the C_{iss}–v_{GS} characteristics changed because the depletion-layer capacitance in the channel region changed significantly [17]. In these enlarged areas, the C_{iss}–v_{GS} characteristics of all DUTs fluctuated along the v_{GS} axis. The parallel fluctuation of the C_{iss}–v_{GS} characteristics along the v_{GS} axis was attributable to the mobile oxide charge and oxide-trapped charges in the gate oxide [118][119].

In addition, Figs. 4.24–4.27 show the i_D–v_{GS} characteristics for DUT–A, DUT–B, DUT–C, and DUT–D, respectively. The i_D–v_{GS} characteristics were measured

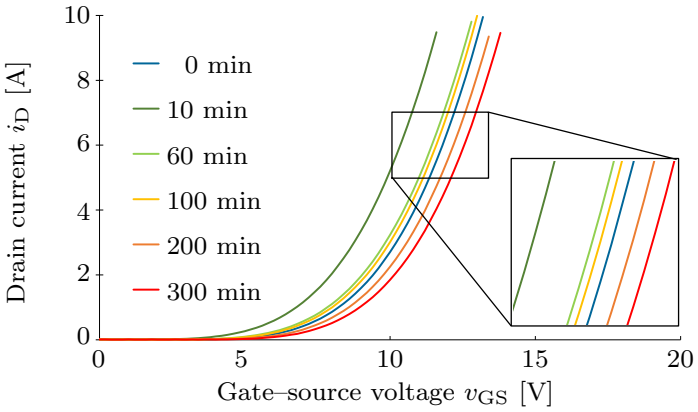


Fig.4.25. i_D–v_{GS} characteristics for DUT–B.

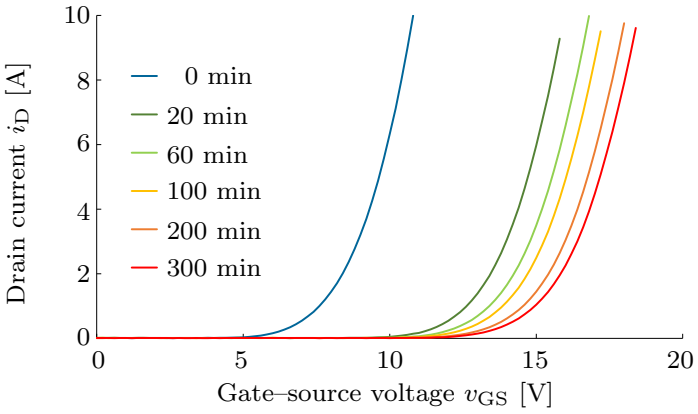


Fig.4.26. i_D–v_{GS} characteristics for DUT–C.

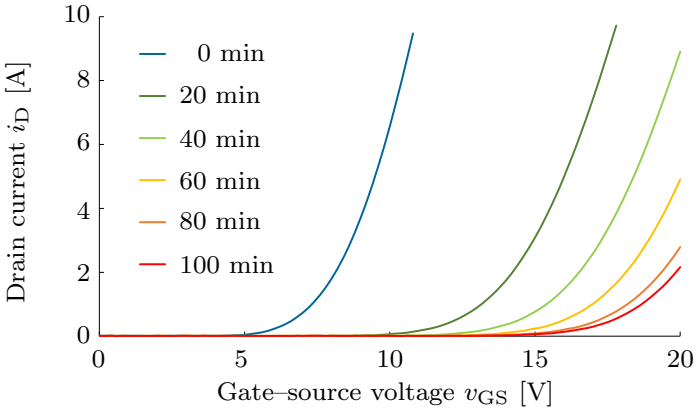


Fig.4.27. i_D–v_{GS} characteristics for DUT–D.

for Sample 1, as shown in Figs. 4.10–4.17 for each DUT. It can be confirmed that the fluctuations in the direction of the v_{GS} axis of the i_D–v_{GS} characteristic resembled the fluctuations in the enlarged area of the C_{iss}–v_{GS} characteristics. Therefore, it is inferred that the surface potential of the gate oxide and threshold

voltage V_{th} fluctuated.

The fluctuation of the on-resistance $R_{\mathrm{DS(ON)}}$ was considered to be caused by the interface-trapped charge at the oxide–semiconductor interface of the channel region. For DUT–C and DUT–D, the fluctuation of the on-resistance $R_{\mathrm{DS(ON)}}$ was large and exceeded the datasheet's guaranteed value. The C_{iss}–v_{GS} characteristics of DUT–C and DUT–D (Figs. 4.22 and 4.23) show both a parallel fluctuation in the v_{GS} axis direction and a stretched fluctuation in the v_{GS} axis direction. The stretched fluctuation in the v_{GS} axis direction was attributable to the interface-trapped charge at the oxide–semiconductor interface [118][119]. Therefore, it is inferred that the defect density at the interface increased and the on-resistance $R_{\mathrm{DS(ON)}}$ fluctuated.

4.3 Discussion on C_{iss}–v_{GS} Characteristics as Aging Precursors

The experimental results in Sections 4.1 and 4.2 confirm the fluctuation of the C_{iss}–v_{GS} characteristics attributable to accelerated aging for the gate oxide of SiC MOSFETs under various conditions and in different types of DUTs. In this section, the results of Sections 4.1 and 4.2 and the experimental verification of the temperature dependence of the C_{iss}–v_{GS} characteristics are presented, to demonstrate experimentally that these characteristics are suitable as aging precursors for condition monitoring.

The temperature dependence of the degradation characteristics of the gate oxide before and after aging was experimentally verified using the advanced HTGB test discussed in Sections 4.1 and 4.2. To clarify the temperature dependence of the degradation characteristics, the static characteristics of the DUTs before and after aging were measured under the conditions of case temperatures $T_{\mathrm{c}} = 25°\mathrm{C}$ and $T_{\mathrm{c}} = 150°\mathrm{C}$, respectively. The DUT was an SiC MOSFET (C2M0280120D, Cree), and the detailed specifications are summarized in Tab. 4.1. The test conditions

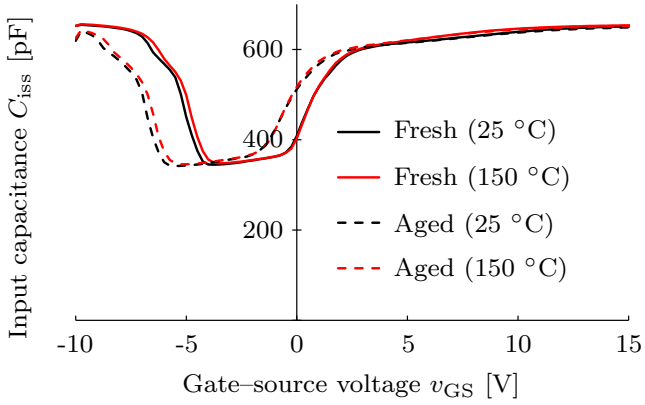


Fig.4.28. Degradation and temperature dependence of C_{iss}–v_{GS} characteristics.

for the advanced HTGB test matched the test condition iii) described in Section 4.1. However, the test duration was set to 30 minutes.

Fig. 4.28 shows the measurement results of the C_{iss}–v_{GS} characteristics. From Fig. 4.28, a characteristic fluctuation can be observed where the C_{iss}–v_{GS} characteristic shifts parallel to the v_{GS} axis under degradation, whilst the characteristic fluctuation attributable to temperature is almost negligible. The C_{iss}–v_{GS} characteristics show a maximum parallel shift of 2.5 V in the negative direction of the v_{GS} axis, attributable to degradation. Assuming that this fluctuation is due to the change in the oxide charge Q_{ox}, the defect density can be calculated. The oxide charge Q_{ox} change entailed by accelerated aging is given by the following equation:

$$\begin{aligned} Q_{\mathrm{ox}} &= C_{\mathrm{ox}} \times 2.5 \text{ V} \\ &= 650 \text{ pF} \times 2.5 \text{ V} \\ &= 1.63 \text{ nC}. \end{aligned} \tag{4.2}$$

The area of the gate oxide S_{ox} is given by

$$C_{\mathrm{oc}} = \varepsilon_{\mathrm{ox}} \frac{S_{\mathrm{ox}}}{t_{\mathrm{ox}}}, \tag{4.3}$$

where $\varepsilon_{\mathrm{ox}}$ is the dielectric constant of the oxide and t_{ox} is the oxide thickness. Because the oxide thickness of the DUT used is 63 nm, $S_{\mathrm{ox}} = 1.19 \times 10^{-2}$ cm^2 [46]. Therefore, assuming that the oxide charge Q_{ox} is distributed over the sheet, the oxide charge density is calculated to be 2.3×10^{12} cm^{-2}. The defect density of

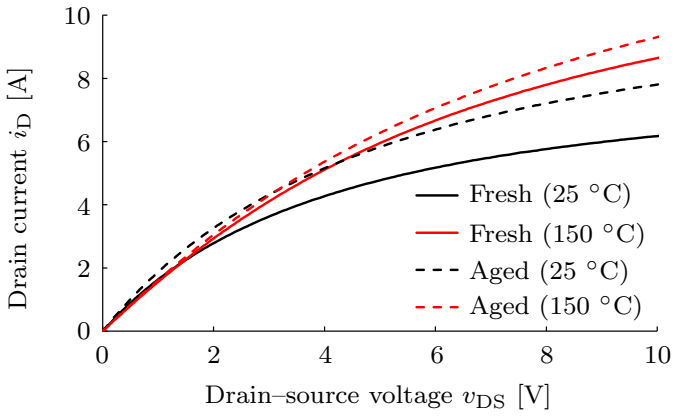


Fig.4.29. Degradation and temperature dependence of i_D–v_{DS} characteristics ($v_{GS} = 10$ V).

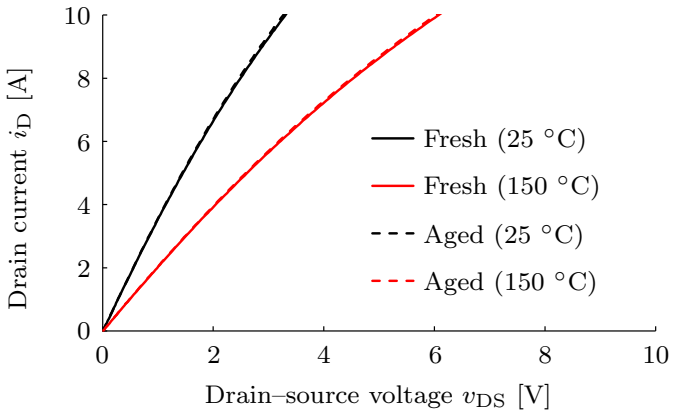


Fig.4.30. Degradation and temperature dependence of i_D–v_{DS} characteristics ($v_{GS} = 20$ V).

SiC MOSFETs has been reported to be of the order of 10^{11}–10^{12} in general, equal to the change in oxide charge density. Therefore, the characteristic fluctuation is considered to have occurred as a result of the oxide charge.

For comparison, Fig. 4.29 shows the measurement results of drain current i_D verses drain–source voltage v_{DS} characteristics (i_D–v_{DS} characteristics) at a gate–source voltage of $v_{GS} = 10$ V. From Fig. 4.29, we seen that both the characteristic fluctuation due to temperature and degradation are clear. Fig. 4.30 shows the measurement results of the i_D–v_{DS} characteristics at the gate–source voltage $v_{GS} = 20$ V. Fig. 4.30 shows that the characteristic fluctuation attributable to temperature is obvious, whilst the characteristic fluctuation due to degradation is almost negligible.

From the above measured results of the C_{iss}–v_{GS} and i_D–v_{DS} characteristics, it is

concluded that the theoretical study in Section 2.2 can be experimentally demonstrated. Therefore, it is experimentally shown that the C_{iss}–v_{GS} characteristic is suitable as an aging precursor for condition monitoring.

4.4 Summary

In this chapter, accelerated aging tests were performed to experimentally verify the degradation characteristics of SiC MOSFETs using the accelerated aging test method and circuit (the advanced HTGB test) developed in Chapter 3. From the results of the accelerated aging tests, the gate oxide degradation of SiC MOSFETs was discussed, and the theoretical considerations in Section 2.2 were experimentally verified.

In the advanced HTGB test employing one type of SiC MOSFET as the DUT, the experimental results show that the degradation trend differed under different test conditions. Furthermore, in the advanced HTGB test for four types of SiC MOSFETs as DUTs, it was found that the degradation tendencies between samples of the same type were identical, though the degradation tendency differed for different DUTs. These results suggest that when developing a condition monitoring technology for power devices, it is necessary to perform accelerated aging tests of power devices under conditions close to those of actual use.

The temperature dependence of the degradation characteristics of SiC MOSFETs under accelerated aging of the gate oxide was verified by experiments. The experimental results show that the temperature dependences of the C_{iss}–v_{GS} characteristics were sufficiently small compared to the degradation characteristics. These results suggest that the C_{iss}–v_{GS} characteristics are suitable as an aging precursor for condition monitoring.

Chapter 5

Measurement Circuit for Condition Monitoring

To establish a condition-based maintenance technology for power devices, a measurement circuit is needed to detect degradation. The measurement circuit measures the aging precursor of power devices implemented in power conversion circuits. In this chapter, a measurement circuit is proposed that can measure the C_{iss}–v_{GS} characteristics, which are the aging precursor of the gate oxide specified in the previous discussions. Furthermore, the experimental verification shows that the measurement circuit can measure the fluctuation of the C_{iss}–v_{GS} characteristic produced by gate oxide degradation.

5.1 Measurement Method of C_{iss}–v_{GS} Characteristics

In this section, the established methods for measuring the C_{iss}–v_{GS} characteristic of power devices is reviewed. Based on the features of these measurement methods and the perspective of a measurement circuit to be implemented in power conversion circuits, a suitable measurement method is identified.

5.1.1 High-Frequency Method

The "high-frequency measurement method" is generally used to measure the C_{iss}–v_{GS} characteristics of power devices [120][121]. The high-frequency measurement method is described in international standards as a method to measure the C_{iss}–v_{GS} characteristics of power devices. Fig. 5.1 shows the circuit diagram for

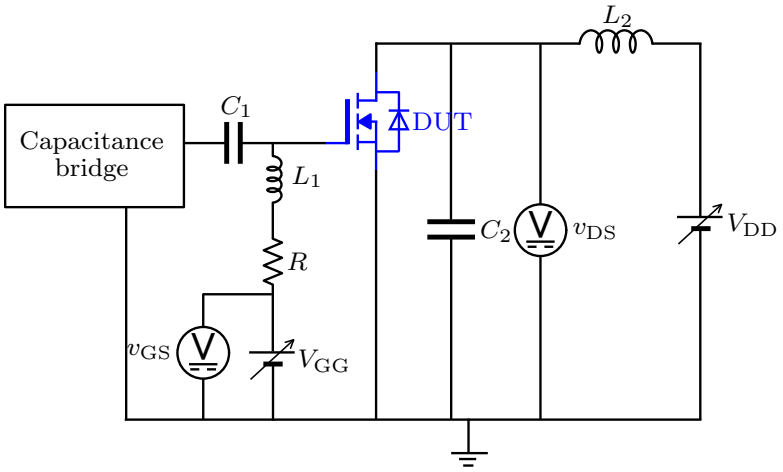


Fig.5.1. C_{iss}–v_{GS} characteristics measurement circuit using high-frequency measurement method [101].

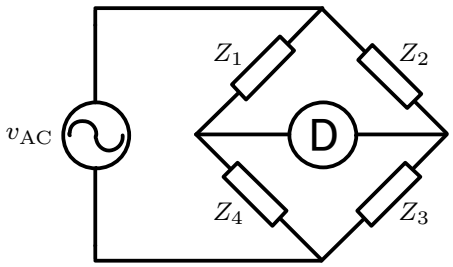


Fig.5.2. Impedance measurement circuit diagram using AC bridge.

measuring the C_{iss}–v_{GS} characteristic [101]. The C_{iss}–v_{GS} characteristic is obtained by setting a variable DC power supply $V_{DD} = 0$ V and measuring the input capacitance C_{iss} using a capacitance bridge (AC bridge) whilst changing the value of V_{GG}.

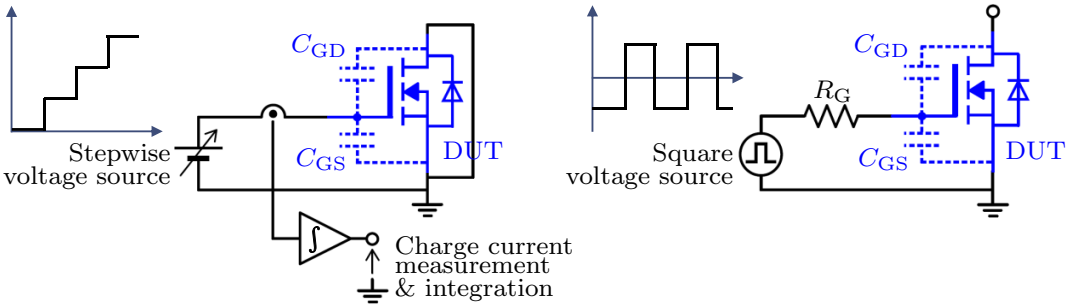
Fig. 5.2 shows an impedance measurement circuit diagram using an AC bridge. In the circuit shown in Fig. 5.2, the equilibrium condition for the Detector D pointing to zero is

$$\begin{cases} R_1R_3 - X_1X_3 = R_2R_4 - X_2X_4 \\ R_1X_3 + R_3X_1 = R_2X_4 + R_4X_2, \end{cases}$$

when

$$Z_i = R_i + jX_i \quad (i = 1,\ 2,\ 3,\ 4). \tag{5.1}$$

From the above equations, if three impedances are known, the unknown impedance can be calculated [122].



(a) Quasi-static method (b) Conventional gate drive circuit

Fig.5.3. Comparison of measurement circuit using quasi-static method and conventional gate drive circuit.

However, it is difficult to implement the functions required for C_{iss}–v_{GS} characteristic measurements when using the high-frequency method in a power conversion circuit.

5.1.2 Quasi-Static Method

In this study, the quasi-static method (charge–voltage method) was adopted as the measurement method for the C_{iss}–v_{GS} characteristic, because its configuration for the measurement is similar to that of the gate drive circuit, and its measurement function can be implemented in that circuit. Fig. 5.3 shows a comparison of the measurement circuit using the quasi-static method and conventional gate drive circuit. As shown in Fig. 5.3(a), the measurement of C_{iss}–v_{GS} characteristics using the quasi-static method requires a stepwise voltage source and current sensor, to measure the charging current to the input capacitance C_{iss}. On the other hand, the conventional gate drive circuit requires a square voltage source for the gate drive, as shown in Fig. 5.3(b). Furthermore, it is possible to measure the charging current to the input capacitance C_{iss} using the gate resistor R_{G} as a shunt resistor.

Fig. 5.4 demonstrates the principle of measuring the C_{iss}–v_{GS} characteristics using the quasi-static method (charge–voltage method). v_{G} and v_{out} in Fig. 5.4 represent the output voltage of the stepwise voltage source and integrator, respectively, as shown in Fig. 5.3(a). In the quasi-static method (charge–voltage

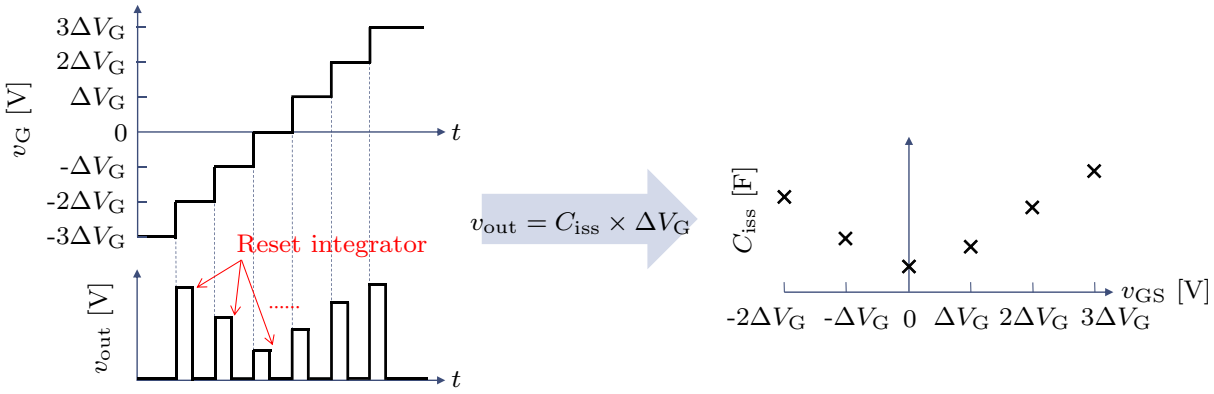


Fig.5.4. Outline of the measurement principle under the quasi-static method (charge–voltage method).

method), the following procedure is used to measure the C_{iss}–v_{GS} characteristics:

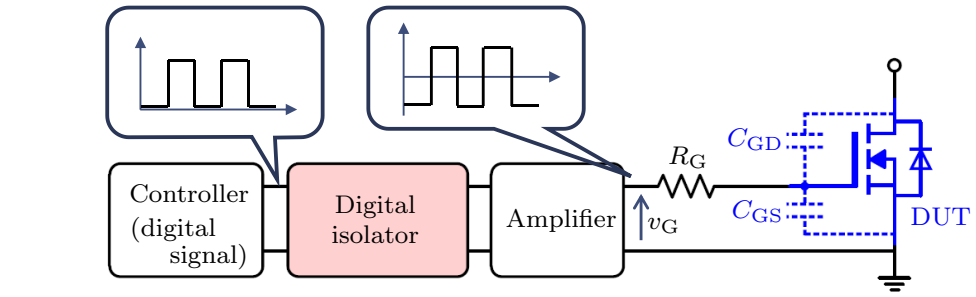
1. The output voltage v_G of the stepwise voltage source is changed using the voltage width ΔV_G.
2. The current sensor measures the charging current to the input capacitance C_{iss}.
3. The charge current is integrated by the integrator, and v_{out} is outputted therefrom.
4. The input capacitance C_{iss} is calculated from the output voltage v_{out} of the integrator.
5. The integrator is reset.

By repeating the above procedure, the C_{iss}–v_{GS} characteristics of the DUT can be measured.

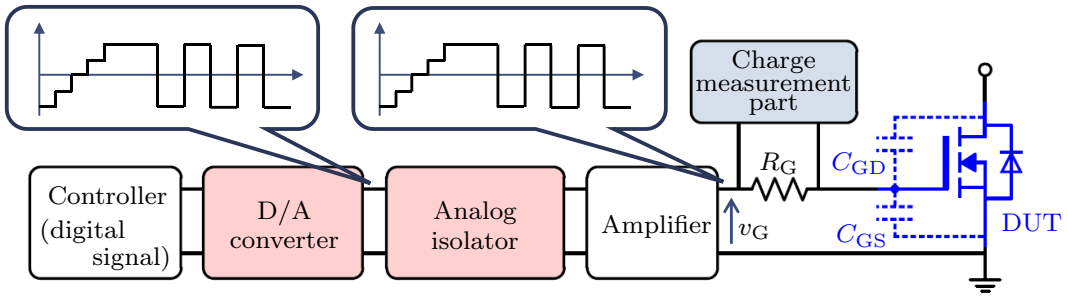
5.2 Gate Drive Circuit with *In-situ* Measurement Function of C_{iss}–v_{GS} Characteristics

5.2.1 Design Method of the Proposed Circuit

In this study, the C_{iss}–v_{GS} characteristic measurement function using the quasi-static method was added to the gate drive circuit. Fig. 5.5 shows the configuration



(a) Conventional gate drive circuit



(b) Proposed gate drive circuit

Fig.5.5. Comparison of conventional and proposed gate drive circuits.

of a conventional and proposed gate drive circuit. In the conventional gate drive circuit [as shown in Fig. 5.5(a)], the binary signal (Hi or Lo) output from the controller is isolated by a digital isolator. The output of the digital isolator is amplified to the power required to drive the gate of the DUT. The measurement of C_{iss}–v_{GS} characteristics using the quasi-static method described in Section 5.1.2 requires the stepwise voltage source to apply a stepwise voltage to the gate–source. Therefore, in the proposed gate drive circuit shown in Fig. 5.5(b), the digital signal output from the controller is converted to an analog signal using a digital-to-analog converter (D/A converter). The analog signal is isolated by an analog isolator and amplified to the power required to drive the gate of the DUT. Under this configuration, v_{G} can output both the square voltage required to drive the DUT gate and the stepwise voltage required to measure the C_{iss}–v_{GS} characteristic.

Fig. 5.6 shows the circuit diagram of the proposed gate drive circuit. The circuit shown in Fig. 5.6 can be divided into a “gate driver part” that outputs the stepwise voltage and a “charge measurement part” that measures the charge charged in the

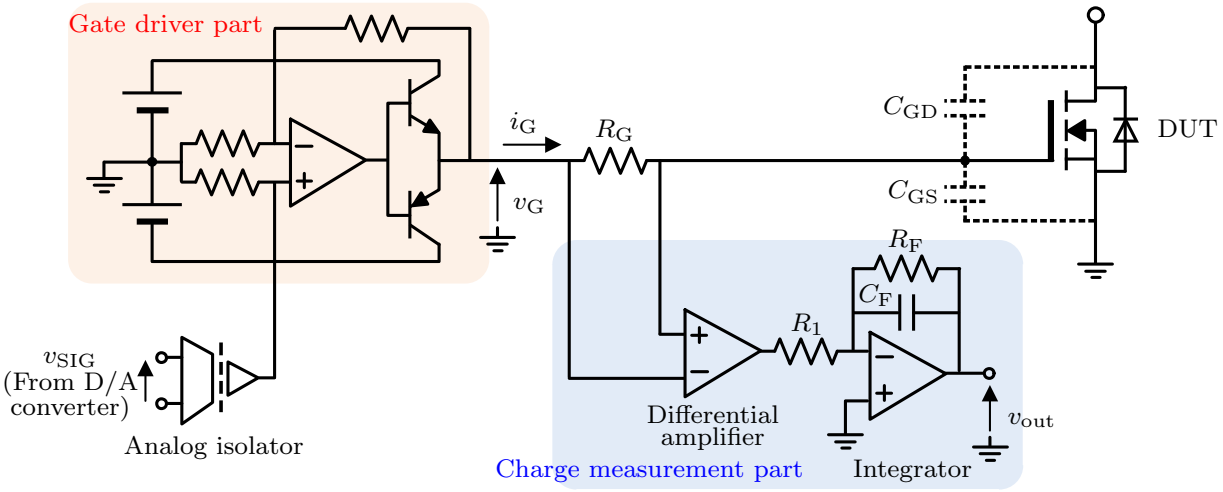


Fig.5.6. Circuit diagram of the proposed gate drive circuit.

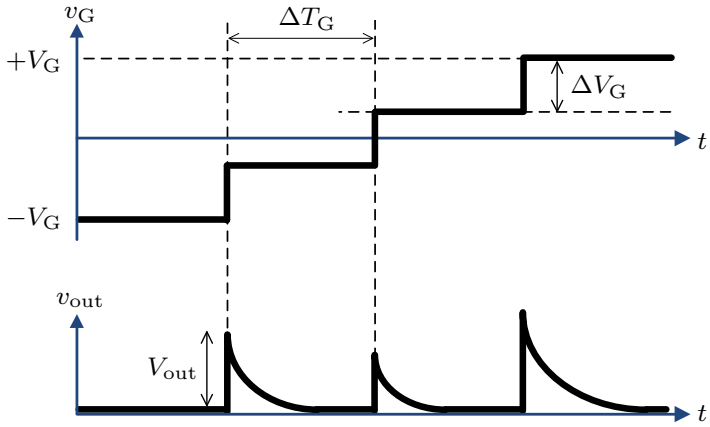
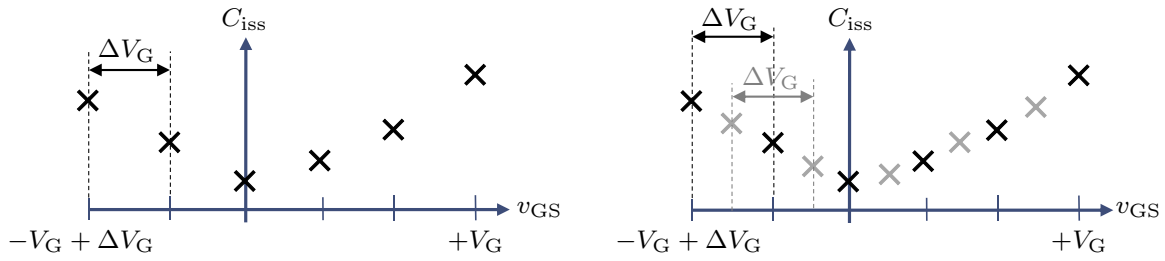


Fig.5.7. Schematic waveforms of the output voltages for the gate driver and charge measurement parts.

input capacitance C_{iss}. The analog output signal v_{SIG} is isolated by the analog isolator and inputted to the gate driver part. The gate driver part amplifies the input signal using a push-pull circuit in the same way as the conventional gate drive circuit. The charge charged to the input capacitance C_{iss} of the DUT is calculated by measuring the voltage across the gate resistance R_G in the charge measurement part. Fig. 5.7 presents schematic waveforms of the output voltage of the gate driver v_G and charge measurement v_{out} parts.

First, the design of the gate driver part is described. The specifications of the stepwise voltage outputted from the gate driver part should be designed consider-



(a) Without function (b) With function

Fig.5.8. C_{iss}–v_{GS} characteristic with and without the gate–source voltage resolution improvement method.

ing the specifications of the C_{iss}–v_{GS} characteristics to be measured. Fig. 5.8(a) shows the specification of the C_{iss}–v_{GS} characteristic measured by the stepwise voltage shown in Fig. 5.7. The measured gate–source voltage range ($-V_{\mathrm{G}}+\Delta V_{\mathrm{G}} \leq v_{\mathrm{GS}} \leq +V_{\mathrm{G}}$) and DC bias width ($\Delta V_{\mathrm{G}}$) of the C_{iss}–v_{GS} characteristic are determined by the minimum stepwise voltage $-V_{\mathrm{G}}$, maximum stepwise voltage $+V_{\mathrm{G}}$, and voltage width of the stepwise voltage ΔV_{G}. If the gate–source voltage resolution is to be improved, the DC bias width (i.e., the voltage width ΔV_{G}) needs to be smaller. However, if the voltage width is smaller, the error from the ideal stepwise voltage becomes larger, owing to the decrease in the voltage change rate. Moreover, the error in the measured C_{iss}–v_{GS} characteristic also increases. Therefore, Fig. 5.8(b) shows the method of improving the gate–source voltage resolution whilst maintaining the voltage width ΔV_{G} of the stepwise voltage. From Fig. 5.8(b) (e.g., when $\Delta V_{\mathrm{G}} = 1$ V), the stepwise voltage was varied in a stepwise manner from -15, -14, -13,..., 13, 14, 15 V to -14.5, -13.5, -12.5,..., 12.5, 13.5, 14.5 V. In this manner, the gate–source voltage resolution was improved without changing the voltage width ΔV_{G}.

Next, the design of the charge measurement part is described. When the output voltage of the gate driver part v_{G} changes stepwise by ΔV_{G}, the output voltage of the charge measurement part V_{out} is given by

$$V_{\mathrm{out}} = \frac{G R_{\mathrm{G}} C_{\mathrm{iss}} \Delta V_{\mathrm{G}}}{R_1 C_{\mathrm{F}}}, \tag{5.2}$$

where G is the gain of the differential amplifier. As shown in Eq. 5.2, when the output voltage of the gate driver part v_{G} changes stepwise, the charge measurement part outputs V_{out}, proportional to the charge charged in the input capacitance C_{iss}. The output voltage of the charge measurement part v_{out} gradually decreased as the charge charged in the capacitor of the integrator C_{F} was discharged by the resistor R_{F}. If the time constant $R_{\mathrm{G}}C_{\mathrm{iss}}$ is sufficiently small and the charging time of the input capacitance C_{iss} is neglected, the output voltage of the charge measurement part $V_{\mathrm{out}}(t)$ at time t after the stepwise voltage changes are given by the following equation:

$$V_{\mathrm{out}}(t) = V_{\mathrm{out}} \exp\left(-\frac{t}{R_{\mathrm{F}}C_{\mathrm{F}}}\right). \tag{5.3}$$

From Eq. 5.3, and by setting the time width of the stepwise voltage ΔT_{G} longer than the time in which the capacitor of the integrator C_{F} is sufficiently discharged, a reset circuit for the integrator (using a switch) is unnecessary.

5.2.2 Operation Sequence

When measuring the C_{iss}–v_{GS} characteristic of the DUT via the proposed gate drive circuit, the drain–source voltage of the DUT must be set to $v_{\mathrm{DS}} = 0$ V. Therefore, the gate drive circuit is suitable for power conversion circuits in which the main circuit and power supply can be opened by a contactor. In this study, it was considered that the condition monitoring of the DUT was performed when the main circuit was not operating in a power conversion circuit with such a circuit configuration.

Fig. 5.9 shows a schematic diagram of a typical buck converter circuit implemented in the proposed condition monitoring system. Fig. 5.10 shows the operation sequence during startup in the circuit shown in Fig. 5.9. In the dormant power conversion circuit, the main circuit is disconnected from the power supply by the contactor, and the input voltage of the main circuit is $v_{\mathrm{IN}} = 0$ V. Before the DC voltage E is applied to the main circuit, the control circuit including

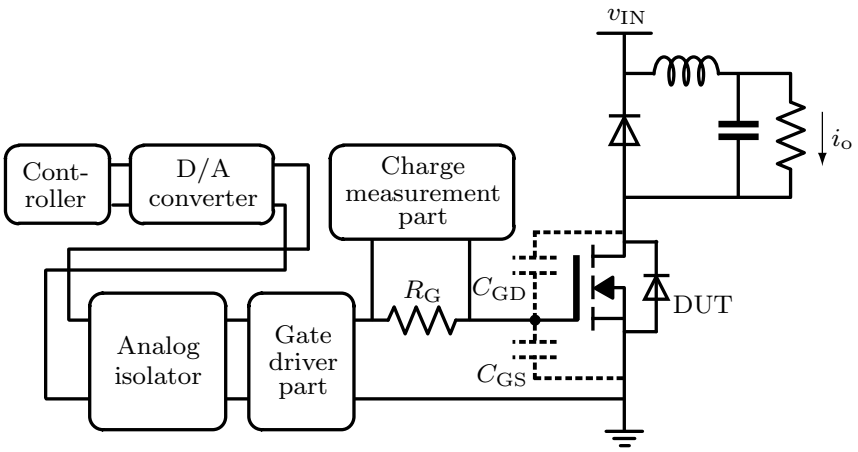


Fig.5.9. Schematic diagram of the proposed condition monitoring system in a typical buck converter.

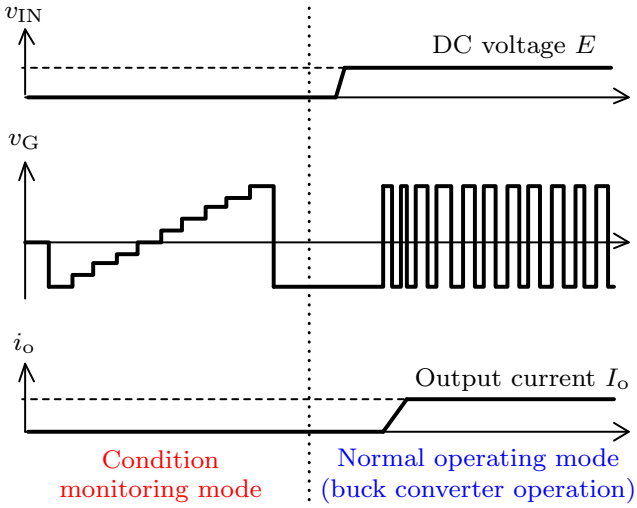


Fig.5.10. Operation sequence of the proposed gate drive circuit.

the gate drive circuit is activated. At that time, as shown in Fig. 5.10, the gate drive circuit outputs the stepwise voltage as the "condition monitoring mode" and measures the C_{iss}–v_{GS} characteristic. After that, the DC voltage E is applied to the main circuit, and the gate drive circuit outputs the square voltage as the "normal operating mode." In the normal operating mode, the operation matches that of a conventional buck converter circuit. In the proposed operation sequence, the condition monitoring is performed when the main circuit is not operational; therefore, the C_{iss}–v_{GS} characteristic can be measured without being affected by electromagnetic noise from the main circuit.

Fig.5.11. Prototype of the gate drive circuit.

Furthermore, in a circuit configuration where MOSFETs are connected in series (e.g., in the leg of an inverter circuit), condition monitoring can be performed by turning off one MOSFET and setting the drain–source voltage of the other MOSFET to $v_{\mathrm{DS}} = 0$ V.

5.2.3 Experimental Verification

It is experimentally verified that the proposed gate drive circuit can monitor the condition of the C_{iss}–v_{GS} characteristic and drive the gate of the power devices. Fig. 5.11 shows the experimental circuit. Fig. 5.12 shows the circuit diagram of the gate drive circuit used in the experiment. Tab. 5.1 summarizes the part numbers and parameters used in the experimental circuit. In addition, Tab. 5.2 summarizes the specifications of the output voltage of the gate driver part v_{G} in the condition monitoring and normal operating modes. The maximum output voltage of the gate driver part was set to 15 V, and the minimum output voltage was set to -15 V. The voltage width of the stepwise voltage ΔV_{G} in the condition monitoring mode was set to 1 V, and the time width ΔT_{G} was set to 100 μs. The square voltage in the normal operating mode was set to ± 15 V, 20 kHz (the on-duty ratio was 0.5).

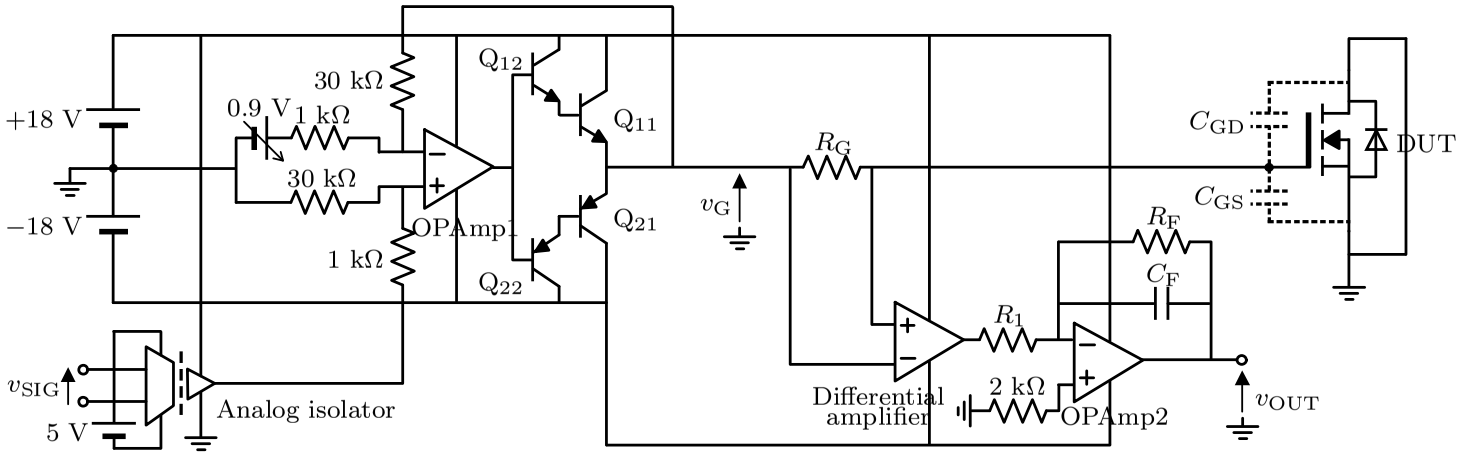


Fig.5.12. Circuit diagram of the gate drive circuit used in the experiment.

Table.5.1 Part numbers and parameters used in the experimental circuit.

Parameters	Value
Analog isolator	ADuM3190
OPAmp1, 2	ADA4625-1
Differential amplifier	AD8421
$\mathrm{Q}_{11}, \mathrm{Q}_{12}$	2SC5866
$\mathrm{Q}_{21}, \mathrm{Q}_{22}$	2SA2094
Gate resistance R_{G}	56 Ω
Gain of instrumentation amplifier G	20
Resistance R_1	2 kΩ
Resistance R_{F}	20 kΩ
Capacitance C_{F}	1 nF

Table.5.2 Specification of output voltage for gate driver part v_{G}

Parameters	Condition monitoring	Normal operating
Maximum voltage	15 V	15 V
Minimum voltage	−15 V	−15 V
Voltage width ΔV_{G}	1 V	–
Time width ΔT_{G}	100 μs	25 μs (20 kHz)

Fig. 5.13 shows the experimental waveforms of the output voltage of the gate driver v_{G} and charge measurement v_{out} parts. The experimental waveforms shown in Fig. 5.13 were averaged 1,000 times using the averaging function of the oscilloscope, to remove aperiodic noise. In the condition monitoring mode, the gate driver part produced the stepwise voltage according to the specifications. The output voltage of the charge measurement part v_{OUT} was outputted according to the change in the stepwise voltage.

Fig. 5.14 shows the calculation results of the C_{iss}–v_{GS} characteristics monitored by the gate drive circuit. In Fig. 5.14, the results of condition monitoring using that gate drive circuit are shown with crosses, and the results of measurement using the high-voltage CV measurement system (CS-603A, Iwatsu) are shown with solid lines. The measurement conditions using the high-voltage CV measurement system were as follows: the measurement signal was $v_{\mathrm{AC}} = 25$ mV (1 MHz), the DC bias width was 0.25 V, and the measurement time was "Medium." The purpose of this experiment was to verify the basic operation; hence, the output voltage V_{out} of the charge measurement part was measured using an oscilloscope. Based on the measured V_{out}, the input capacitance C_{iss} was calculated using Eq. 5.2. From Fig. 5.14, it can be seen that the C_{iss}–v_{GS} characteristic of the condition monitoring was generally consistent with those measured by the high-voltage CV measurement system. It can also be seen that the fluctuations attributable to degradation could be measured by condition monitoring.

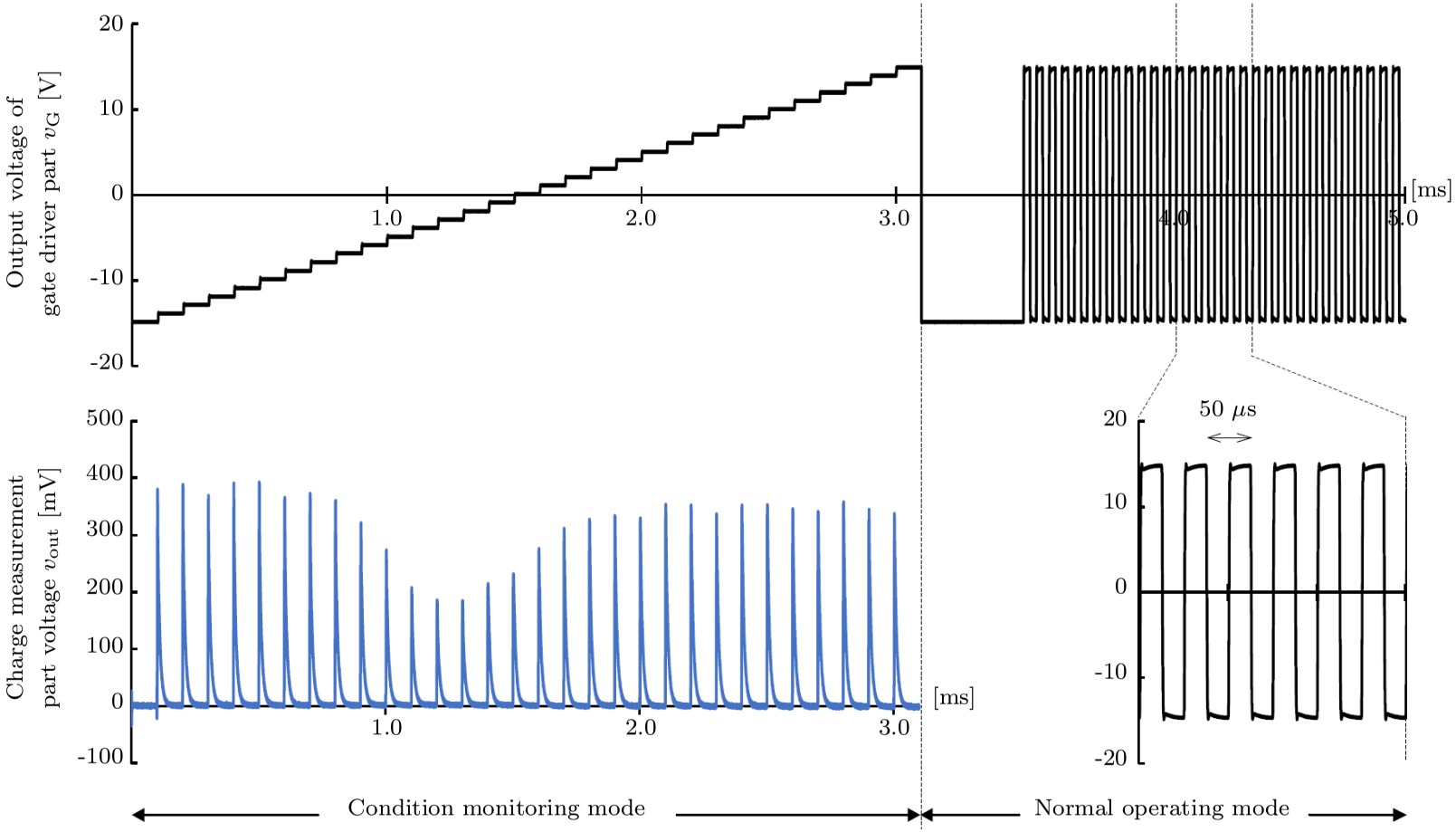


Fig.5.13. Experimental waveforms of the proposed gate drive circuit.

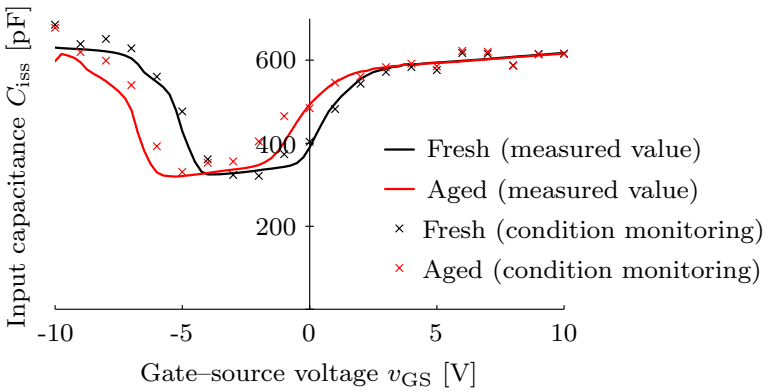


Fig.5.14. Comparison of the C_{iss}–v_{GS} characteristics between the measured values and condition monitoring (without the gate–source voltage resolution improvement method).

Fig. 5.15 shows the result of applying the gate–source voltage resolution improvement method to condition monitoring using the gate drive circuit. The gate–source voltage resolution can be seen to be improved compared to Fig. 5.14, although the DC bias width of 1 V remains the same. The results also show that the C_{iss}–v_{GS} characteristic of the condition monitoring is generally consistent with those measured by the high-voltage CV measurement system.

On the other hand, Fig. 5.14 shows that in the region where the input capacitance C_{iss} changes significantly with respect to the gate–source voltage v_{GS}, the error between the value measured by the high-voltage CV measurement system and that obtained through condition monitoring tends to be large. This measurement error is thought to be caused by the fact that a part of the charge in the semiconductor takes time to follow the change in DC bias. Fig. 5.16 shows the results of measuring the C_{iss}–v_{GS} characteristics of the fresh DUT under different sweep conditions of the DC bias. In Fig. 5.16, the area of $v_{\mathrm{GS}} \leqq 0$, where the measurement error was particularly large in Fig. 5.14, is shown enlarged. In the measurement by the high-voltage CV measurement system, the DC bias sweep was set in the positive direction. In the measurement by the high-voltage CV measurement system in Fig. 5.14, the DC bias width was 0.25 V and the measurement time was set to “Medium” as the DC bias sweep conditions. On the other hand, the measurement results shown in blue in Fig. 5.16 were obtained with a

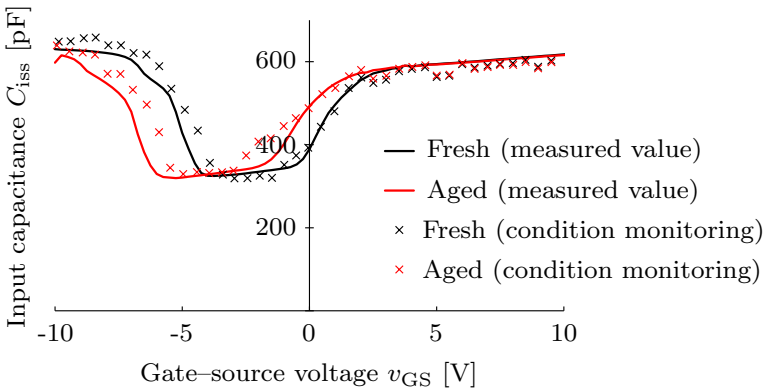


Fig.5.15. Comparison of the C_{iss}–v_{GS} characteristics between the measured values and condition monitoring (with the gate–source voltage resolution improvement method).

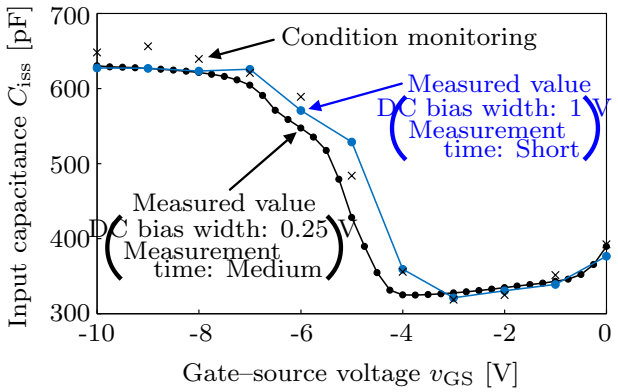


Fig.5.16. C_{iss}–v_{GS} characteristics under different DC bias sweep conditions (Fresh DUT).

DC bias width of 1 V and a measurement time set to "Short," because the sweep conditions of the DC bias (the measurement time cannot be set in absolute values because it depends on the time required for GPIB/USB communication and screen display, though "Short" has a shorter measurement time than "Medium"). In other words, because the voltage change of DC bias is large and the measurement time is short, the charge that requires time to follow the change of DC bias is not measured accurately. In the measurement of the C_{iss}–v_{GS} characteristic by condition monitoring, the charge time required to follow the change in DC bias is not accurately calculated because the charging time to the input capacitance C_{iss} is neglected when deriving Eq. 5.3.

5.3 Summary

A gate drive circuit that can measure the C_{iss}–v_{GS} characteristics (proposed as an aging precursor in this study) were developed for condition monitoring of SiC MOSFETs.

First, to select a measurement method for C_{iss}–v_{GS} characteristics, the conventional measurement methods were reviewed. The quasi-static method (charge–voltage method) was selected as a measurement method from the perspective that the measurement function must be implementable in power conversion circuits. Next, the design method of the gate drive circuit and operation sequence was proposed. Finally, experiments using the 1.2 kV SiC MOSFET as the DUT were performed to verify the possibility of monitoring the condition of the C_{iss}–v_{GS} characteristic and driving the gate at 20 kHz. The experimental results demonstrate that the degradation characteristics expressed in the C_{iss}–v_{GS} characteristic can be measured by condition monitoring.

Chapter 6

Conclusions and Future Work

6.1 Conclusion

This dissertation proposed a method for monitoring the gate oxide degradation of SiC MOSFETs, which represent a fundamental technology for realizing the condition-based maintenance of power conversion circuits. The subjects covered and the proposals given in each chapter are described below.

Chapter 2 summarized the relevant previous studies on condition monitoring technology for power devices. From the aging precursor issues that have already been proposed, we clarified that electrical characteristics that fluctuate with respect to degradation and have small temperature dependences are suitable as new aging precursors. Through theoretical studies, it was shown that the C_{iss}–v_{GS} characteristic (a voltage-dependent capacitance) is suitable as an aging precursor.

In Chapter 3, to experimentally verify the theoretical studies in Chapter 2, an accelerated aging method for power devices (and the relevant test circuit) was proposed. The method facilitates the accelerated aging of the gate oxide under similar switching conditions as the power devices implemented in the power conversion circuit. In addition, the design method operates such that the failure does not spread to the test circuit even if the device fails during the test. The validity of the design method was verified in experiments using a 1.2 kV SiC MOSFET as a DUT under 500 V, 50 A or 800 V, 20 A conditions.

In Chapter 4, the accelerated aging test circuit developed in Chapter 3 was used to perform accelerated aging tests for 1.2 kV SiC MOSFET DUTs. From the test results, it was concluded that (when developing condition monitoring

technology for power devices) the accelerated aging test should be performed under conditions similar to those in actual use, because the degradation trends differ depending on the test conditions. From the results of accelerated aging tests, it was experimentally demonstrated that the C_{iss}–v_{GS} characteristics fluctuate with aging and have a small temperature dependence.

In Chapter 5, a gate drive circuit that can measure the C_{iss}–v_{GS} characteristics proposed as the aging precursor in this study was developed to perform condition monitoring. The design method and operation sequence were proposed. Experimental verification using the 1.2 kV SiC MOSFET DUT was performed to verify the possibility of monitoring the condition of the C_{iss}–v_{GS} characteristic and driving the gate at 20 kHz. The experimental results demonstrate that the degradation characteristics expressed in the C_{iss}–v_{GS} characteristic can be measured by condition monitoring.

Through this discussion, a condition monitoring technology for SiC MOSFETs was proposed; it uses the C_{iss}–v_{GS} characteristics as an aging precursor. In addition, a gate drive circuit that can measure the C_{iss}–v_{GS} characteristics was proposed, and the experimental verification of the gate drive circuit was demonstrated.

6.2 Future Works

In this dissertation, the condition monitoring technology for SiC MOSFET gate oxide degradation was proposed, and the main studies were discussed. However, some considerations still need to be taken into account before practical application of the proposed study. In this section, those considerations are described and the prospects of this study are discussed.

- **Further investigation of C_{iss}–v_{GS} characteristic and gate oxide degradation**

  This dissertation has shown that C_{iss}–v_{GS} fluctuates owing to the degradation of the gate oxide. However, further investigation of the

C_{iss}–v_{GS} characteristics and gate oxide degradation is needed. In Section 5.2, charges that required a change in time to follow the change in DC bias during C_{iss}–v_{GS} characteristic measurement were not accurately calculated by the condition monitoring procedure. It is necessary to investigate how these charges are related to the degradation of SiC MOSFETs and to clarify which degradation is detectable under the proposed method. Furthermore, it is necessary to consider the threshold for determining degradation, with respect to the relationship between the occurrence of BTI or TDDB and the fluctuation of C_{iss}–v_{GS}.

The proposed accelerated aging test circuit and C_{iss}–v_{GS} characteristic measurement circuit can be used in combination. The degradation characteristics of SiC MOSFETs can be further analyzed by simultaneously performing accelerated aging and condition monitoring tests.

- **Further investigation of the C_{iss}–v_{GS} characteristic measurement circuit**

  The proposed measurement circuit has a small issue, in that the timing of the condition monitoring is limited. Because the oxide charge may be trapped and de-trapped repeatedly, it is better to monitor the condition several times. Because the C_{iss}–v_{GS} characteristics have a small temperature dependence, a method to monitor the condition whilst the power conversion circuit is still operating may be considered.

- **Digitization of power electronic systems**

  Focusing on the fact that condition monitoring technology has a high affinity with the digitization technology of power electronic systems, the integration of the power electronics field with other fields is being considered. Fig. 6.1 presents a conceptual diagram of digitization technology for power electronic systems [123]. The data measured by sensors in power elec-

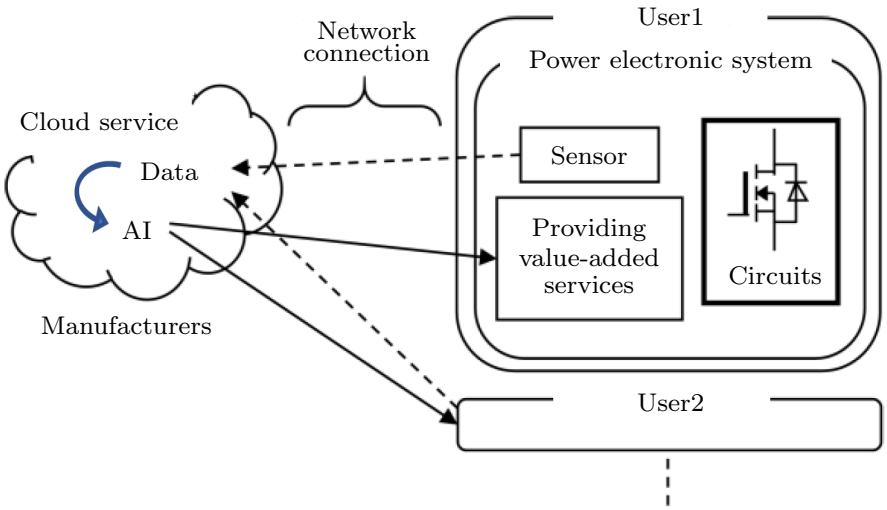


Fig.6.1. Digitization of power electronic systems [123].

tronic systems is collected in a cloud via a network. Manufacturers of these systems or power devices can access the collected information. Obtaining the degradation characteristics of power devices in operational systems is important for clarifying the degradation mechanisms. Because the degradation mechanism of power devices remains unclear in many areas, it is of great academic significance. Furthermore, clarification of the degradation mechanism will facilitate the design of power electronic systems with an appropriate expected lifetime, which will contribute to developments in sustainability.

References

[1] "Realization of a Green Society," Homepage of Prime Minister's Office of Japan, [Online], Available: https://www.kantei.go.jp/jp/headline/tokushu/green.html (in Japanese) (Last viewed on Oct. 27, 2021).

[2] "Green growth strategies associated with carbon-neutral 2050," Growth Strategy Conference Document 2, Ministry of Economy, Trade and Industry, Dec. 2020, [Online], Available: https://www.meti.go.jp/press/2020/12/20201225012/20201225012-2.pdf (in Japanese) (Last viewed on Oct. 27, 2021).

[3] D. Ueshin, "Kintetsu Series 80000 "Hinotori," a new train for the Meihan Limited Express, goes on the press," *Mynavi News*, Nov. 2019, [Online], Available: https://news.mynavi.jp/article/20191119-hinotori80000/ (in Japanese) (Last viewed on Feb. 4, 2022).

[4] Safety, Social and Environmental Report 2017 CSR Report, Keio Corporation, p. 70, 2017, [Online], Available: https://www.keio.co.jp/company/environment/social_environment/pdf/csr2017/keio_2017_03-00.pdf (in Japanese) (Last viewed on Oct. 27, 2021).

[5] A. J. Wileman S. Aslam, and S. Perinpanayagam, "A road map for reliable power electronics for more electric aircraft," *Progress in Aerospace Sciences*, vol. 127, 100739, 2021.

[6] B. Rahrovi and M. Ehsani, "A Review of the More Electric Aircraft Power Electronics," in *Proc. 2019 IEEE Texas Power and Energy Conference (TPEC)*, College Station, TX, USA, Feb. 2019.

[7] J. He, D. Zhang, and D. Torrey, "Recent Advances of Power Electronics

Applications in More Electric Aircrafts," in *Proc. 2018 AIAA/IEEE Electric Aircraft Technologies Symposium (EATS)*, Cincinnati, OH, USA, Jul. 2018.

[8] X. Zhao, J. M. Guerrero, and X. Wu, "Review of aircraft electric power systems and architectures," in *Proc. 2014 IEEE International Energy Conference (ENERGYCON)*, Cavtat, Croatia, May 2014.

[9] K. Yamaguchi, K. Katsura, T. Yamada, and Y. Sato, "High Power Density SiC-Based Inverter with a Power Density of 70kW/liter or 50kW/kg," *IEEJ Journal of Industry Applications*, vol. 8, no. 4, pp. 694-703, 2019.

[10] H. Wang and F. Blaabjerg, "Power Electronics Reliability: State of the Art and Outlook," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 6, pp. 6476-6493, 2021.

[11] X. Jiang, J. Wang, J. Chen, H. Yu, Z. Li, and Z. J. Shen, "Investigation on Degradation of SiC MOSFET under Accelerated Stress in PFC Converter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol.9, no.4, pp. 4299-4310, 2021.

[12] N. Moultif, E. Joubert, M. Masmoudi, and O. Latry, "Characterization of HTRB stress effects on SiC MOSFETs using photon emission spectral signatures," *Microelectronics Reliability*, vol. 76-77, pp. 243-248, 2017.

[13] A. Fayyaz and A. Castellazzi, "High temperature pulsed-gate robustness testing of SiC power MOSFETs," *Microelectronics Reliability*, vol. 55, no. 9-10, pp. 1724-1728, 2015.

[14] Y. Katsu, T. Hosoi, Y. Nanen, T. Kimoto, T. Shimura, and H. Watanabe, "Impact of NO Annealing on Flatband Voltage Instability due to Charge Trapping in SiC MOS Devices," *Materials Science Forum*, vol. 858, pp. 599-602, 2016.

[15] Y. Liu, X. Chen, Z. Zhao, Z. G. Li, C. T. Lu, J. G. Zhang, H. Ye, S. W. Koh, L. G. Wang, and G. Zhang, "SiC MOSFET Threshold-Voltage Instability Under High Temperature Aging," in *Proc. 2018 19th International Confer-*

ence on Electronic Packaging Technology (ICEPT), Shanghai, China, Aug. 2018.

[16] J. P. Kozak, K. D. T. Ngo, D. J. DeVoto, and J. J. Major, "Impact of Accelerated Stress-Tests on SiC MOSFET Precursor Parameters," in *Proc. 2018 Second International Symposium on 3D Power Electronics Integration and Manufacturing (3D-PEIM)*, ShCollege Park, MD, USA, Jun. 2018.

[17] J. Wei, S. Liu, R. Ye, X. Chen, H. Song, W. Sun, W. Su, Y. Liu, F. Lin, and B. Hou, "Interfacial damage extraction method for SiC power MOSFETs based on C-V characteristics," in *Proc. 29th International Symposium on Power Semiconductor Devices and IC's (ISPSD)*, Sapporo, Japan, May. 2017, pp. 359-362.

[18] R. Green, A. Lelis, and D. Habersat, "Application of reliability test standards to SiC Power MOSFETs," in *Proc. 2011 International Reliability Physics Symposium*, Monterey, CA, USA, Apr. 2011.

[19] "Commercialization of inverter systems for trains using full-SiC power modules," MITSUBISHI ELECTRIC Corporation NEWS RELEASE · 郡 ocial No.1312, [Online], Available: `http://www.mitsubishielectric.co.jp/news/2013/pdf/1225.pdf` (in Japanese) (Last viewed on Oct. 28, 2021).

[20] "Research on the Global Market for Power Semiconductors (2020)," Yano Research Institute Ltd., press release, No. 2485, 2020, [Online], Available: `https://www.yano.co.jp/press-release/show/press_id/2485` (in Japanese) (Last viewed on Oct. 28, 2021).

[21] N. Keshmiri, D. Wang, B. Agrawal, R. Hou, and A. Emadi, "Current Status and Future Trends of GaN HEMTs in Electrified Transportation," *IEEE Access*, vol. 8, pp. 70553-70571, 2020.

[22] J. O. Gonzalez and O. Alatise, "Bias temperature instability and condition monitoring in SiC power MOSFETs," *Microelectronics Reliability*, vol. 88-90, pp. 557-562, 2018.

[23] T. Aichinger and P. Friedrichs, "Gate oxide and threshold voltage reliability considerations for SiC MOSFETs," *IEEE Applied Power Electronics Conference 2018*, San Antonio, Texas, USA, Mar. 2018, Industry Presentations.

[24] M. Gurfinkel, J. C. Horst, J. S. Suehle, J. B. Bernstein, Y. Shapira, K. S. Matocha, G. Dunne, and R. A. Beaupre, "Time-Dependent Dielectric Breakdown of 4H–SiC/SiO_2 MOS Capacitors," *IEEE Transactions on Device and Materials Reliability*, vol. 8, no. 4, pp. 635-641, 2008.

[25] C. Miccoli and F. Iucolano, "Study of oxide trapping in SiC MOSFETs by means of TCAD simulations," *Microelectronics Reliability*, vol. 97, pp. 40-43, Jul. 2019.

[26] S. Suzuki, *The Challenge of a Plane That Never Falls* Kyoto: Kagaku-Dojin Publishing Company, INC, 2014 (in Japanese).

[27] Y. Nakazawa, I. Aoyama, and I. Yasuoka, "IEGT Devices to Realize Small, Lightweight, and High-Efficiency Power Converter for Rolling Stock," *Toshiba Review*, vol. 63, no. 11, 2008 (in Japanese).

[28] S. Yang, A. Bryant, P. Mawby, D. Xiang, L. Ran, and P. Tavner, "An Industry-Based Survey of Reliability in Power Electronic Converters," *IEEE Transactions on Industry Applications*, vol. 47, no. 3, pp. 1441-1451, 2011.

[29] S. Pu, E. Ugur, F. Yang, and B. Akin, "*In situ* Degradation Monitoring of SiC MOSFET Based on Switching Transient Measurement," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 6, pp. 5092-5100, 2020.

[30] "SiC Power Semiconductors for the Next-Generation Electric Power Society: Commercialization of Inverters for Rolling Stock," *NEDO PROJECT SUCCESS STORIES*, Feb. 2017, [Online], Available: `https://www.nedo.go.jp/hyoukabu/articles/201706sic/index.html` (in Japanese) (Last viewed on Feb. 6, 2022).

[31] T. Fukuda and M. Okumura, "Efforts to Further Improve Reliability of Electronic Equipment for Rolling Stock," *Railway Research Review*, vol.68, no.7,

pp. 6-9, 2011 (in Japanese).

[32] "Reliability of Power Modules," MITSUBISHI ELECTRIC Corporation, 2019, [Online], Available: `https://www.mitsubishielectric.co.jp/semiconductors/products/pdf/reliability/powermodule_reliability_j.pdf` (in Japanese) (Last viewed on Dec. 11, 2021).

[33] H. Oh, B. Han, P. McCluskey, C. Han, and B. D. Youn, "Physics-of-Failure, Condition Monitoring, and Prognostics of Insulated Gate Bipolar Transistor Modules: A Review," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2413-2426, 2015.

[34] K. Wei, W. Wang, Z. Hu, and M. Du, "Condition Monitoring of IGBT Modules Based on Changes of Thermal Characteristics," *IEEE Access*, vol. 7, pp. 47525-47534, 2019.

[35] T. Taniuchi, T. Matsumoto, T. Ogura, K. Kotani, H. Tai, and H. Takeuchi, *Introduction to Practical Power Electronics, Power Semiconductor Devices* Tokyo, Ohmsha, Ltd., 2016 (in Japanese).

[36] C. Chen, F. Luo, and Y. Kang, "A review of SiC power module packaging: Layout, material system and integration," *CPSS Transactions on Power Electronics and Applications*, vol. 2, no. 3, pp. 170-186, 2017.

[37] H. Lee, V. Smet, and R. Tummala, "A Review of SiC Power Module Packaging Technologies: Challenges, Advances, and Emerging Issues," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 239-255, 2020.

[38] B. Boettge, F. Naumann, R. Klengel, S. Klengel, and M. Petzold, "Packaging material issues in high temperature power electronics," in *Proc. 2013 European Microelectronics Packaging Conference (EMPC)*, Grenoble, France, Sep. 2013.

[39] N. Marenco, M. Kontek, W. Reinert, J. Lingner, and M. Poech, "Copper ribbon bonding for power electronics applications," in *Proc. 2013 European Mi-*

croelectronics Packaging Conference (EMPC), Grenoble, France, Sep. 2013.

[40] "SiC modules with 30% lower switching loss than conventional modules," Hitachi Power Semiconductor Device, Ltd., LD-ES-211496, 2021 (in Japanese).

[41] R. Ouaida, M. Berthou, J. Leon, X. Perpina, S. Oge, P. Brosselard, and C. Joubert, "Gate Oxide Degradation of SiC MOSFET in Switching Conditions," *IEEE Electron Device Letters*, vol. 35, no. 12, pp. 1284-1286, 2014.

[42] T. T. Nguyen, A. Ahmed, T. V. Thang, and J. H. Park, "Gate Oxide Reliability Issues of SiC MOSFETs Under Short-Circuit Operation," *IEEE Transactions on Power Electronics*, vol. 30, no. 5, pp. 2445-2455, 2015.

[43] S. Mbarek, F. Fouquet, P. Dherbecourt, M. Masmoudi, and O. Latry, "Gate oxide degradation of SiC MOSFET under short-circuit aging tests," *Microelectronics Reliability*, vol. 64, pp. 415-418, 2016.

[44] J. Wang and X. Jiang, "Review and analysis of SiC MOSFETs' ruggedness and reliability," *IET Power Electronics*, vol. 13, no. 3, pp. 445-455, 2020.

[45] Y. Mori, D. Hisamoto, N. Tega, M. Matsumura, H. Yoshimoto, A. Shima, and Y. Shimamoto, "Effects of interface properties in SiC MOSFETs on reliability," in *Proc. 2015 IEEE 22nd International Symposium on the Physical and Failure Analysis of Integrated Circuits*, Hsinchu, Taiwan, Jun. 2015.

[46] T. Santini, M. Sebastien, M. Florent, L. V. Phung, and B. Allard, "Gate oxide reliability assessment of a SiC MOSFET for high temperature aeronautic applications," in *Proc. IEEE Energy Conversion Congress and Exposition - Asia (ECCE Asia)*, Melbourne, VIC, Australia, Jun. 2013.

[47] T. Bertelshofer, A. Marz, and M.-M. Bakran, "Modelling parallel SiC MOSFETs: thermal selfstabilisation vs. switching imbalances," *IET Power Electronics*, vol. 12, no. 5, pp. 1071-1078, 2019.

[48] D. Sadik, J. Colmenares, D. Peftitsis, J. Lim, J. Rabkowski, and H. Nee, "Experimental investigations of static and transient current sharing of parallel-connected silicon carbide MOSFETs," in *Proc. 2013 15th European Con-*

ference on Power Electronics and Applications (EPE), Lille, France, Sep. 2013.

[49] M. Rafik, A. P. Nguyen, X. Garros, M. Arabi, X. Federspiel, and C. Diouf, "AC TDDB extensive study for an enlargement of its impact and benefit on circuit lifetime assessment," in *Proc. 2018 IEEE International Reliability Physics Symposium (IRPS)*, Burlingame, CA, USA, Mar. 2018.

[50] V. Mulpuri and S. Choi, "Degradation of SiC MOSFETs with gate oxide breakdown under short circuit and high temperature operation," in *Proc. 2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, USA, Oct. 2017, pp. 2527-2532.

[51] A. Bezza, M. Rafik, D. Roy, X. Federspiel, P. Mora, and G. Ghibaudo, "Frequency dependence of TDDB & PBTI with OTF monitoring methodology in high-k/metal gate stacks," in *Proc. 2014 IEEE International Reliability Physics Symposium*, Waikoloa, HI, USA, Jun. 2014.

[52] Y. Q. Chen, X. B. Xu, Y. D. Lu, S. J. Pan, and X. B. Xu, "A prognostic circuit for time-dependent dielectric breakdown failure of MOSFET," in *Proc. 2014 10th International Conference on Reliability, Maintainability and Safety (ICRMS)*, Guangzhou, China, Aug. 2014, pp.944-947.

[53] C. L. Chen, S. W. Chang, S. C. Chen, Y.-H. Lee, Y. W. Lee, D. S. Huang, J. R. Shih, and K. Wu, "The physical mechanism investigation of AC TDDB behavior in advanced gate stack," in *Proc. 2014 IEEE International Reliability Physics Symposium*, Waikoloa, HI, USA, Jul. 2014.

[54] K. T. Lee, J. Nam, M. Jin, K. Bae, J. Park, L. Hwang, and J. Kim; Hyunjin Kim; Jongwoo Park, "Frequency dependent TDDB behaviors and its reliability qualification in 32nm high-k/metal gate CMOSFETs," in *Proc. 2011 International Reliability Physics Symposium*, Monterey, CA, USA, Apr. 2011.

[55] J. Hagiwara, "Preventive Maintenance Ensuring Reliability of Electrical

Equipment for Rolling Stock," *Toshiba review*, vol. 71, no. 4, pp. 40-43, 2016 (in Japanese).

[56] M. Nanbu, "Status of recent facility maintenance initiatives," *Meiden news report*, vol. 353, no. 4, pp. 71-75, 2016 (in Japanese).

[57] K. Hasegawa, S. Nishizawa, and I. Omura, "A Condition-Monitoring Method of DC-Link Capacitors Used in a High-Power Three-Phase PWM Inverter with an Evaluation Circuit," *IEEJ Journal of Industry Applications*, vol. 8, no. 3, pp. 480-487, 2018.

[58] M. Kondo, "Large-Scale Data Learning Method for Anomaly Detection using Machine Learning for Monitoring Vibration in Vehicle Equipment," *IEEJ Transactions on Industry Applications*, vol. 140, no. 6, pp. 480-487, 2019 (in Japanese).

[59] Y. Kudo, M. Suzuki, and T. Kobayashi, "Method for Measurement of Deterioration Level of Electronic Interlocking Equipment Parts," *IEEJ Transactions on Industry Applications*, vol. 138, no. 6, pp. 475-480, 2018 (in Japanese).

[60] M. Ogino, H. Tsunashima, K. Yanagisawa, H. Mori, A. Asano, and S. Wakai, "Development of Track Condition Monitoring System Based on Compact Onboard Sensing Devices," *IEEJ Transactions on Industry Applications*, vol. 135, no. 4, pp. 395-402, 2015 (in Japanese).

[61] S. Zhao, Y. Peng, F. Yang, E. Ugur, B. Akin, and H. Wang, "Health State Estimation and Remaining Useful Life Prediction of Power Devices Subject to Noisy and Aperiodic Condition Monitoring," *IEEE Transactions on Instrumentation and Measurement*, vol. 70, pp. 1-16, 2021.

[62] E. Ugur, F. Yang, S. Pu, S. Zhao, and B. Akin, "Degradation Assessment and Precursor Identification for SiC MOSFETs Under High Temp Cycling," *IEEE Transactions on Industry Applications*, vol. 55, no. 3, pp. 2858-2867, 2019.

[63] Y. Peng and H. Wang, "A Simplified On-State Voltage Measurement Circuit for Power Semiconductor Devices," *IEEE Transactions on Power Electronics*, vol. 36, no. 10, pp. 10993-10997, 2021.

[64] Y. Chen and D. B. Ma, "Self-Aging-Prognostic GaN-Based Switching Power Converter Using TJ-Independent Online Condition Monitoring and Proactive Temperature Frequency Scaling," *IEEE Transactions on Power Electronics*, vol. 36, no. 5, pp. 5022-5031, 2021.

[65] S. Roy, A. Hanif, and F. Khan, "Aging Detection and State of Health Estimation of Live Power Semiconductor Devices Using SSTDR Embedded PWM Sequence," *IEEE Transactions on Power Electronics*, vol. 36, no. 5, pp. 4991-5005, 2021.

[66] S. Zhao, S. Chen, F. Yang, E. Ugur, B. Akin, and H. Wang, "A Composite Failure Precursor for Condition Monitoring and Remaining Useful Life Prediction of Discrete Power Devices," *IEEE Transactions on Industrial Informatics*, vol. 17, no. 1, pp. 688-698, 2021.

[67] C. Bhargava, P. K. Sharma, M. Senthilkumar, S. Padmanaban, V. K. Ramachandaramurthy, Z. Leonowicz, F. Blaabjerg, and M. Mitolo, "Review of Health Prognostics and Condition Monitoring of Electronic Components," *IEEE Access*, vol. 8, pp. 75163-75183, 2020.

[68] M. Schubert and R. W. D. Doncker, "Semiconductor Temperature and Condition Monitoring Using Gate-Driver-Integrated Inverter Output Voltage Measurement," *IEEE Transactions on Industry Applications*, vol. 56, no. 3, pp. 2894-2902, 2020.

[69] F. G.-Hernando, J. S.-Sebastian, A. G.-Bediaga, M. Arias, F. Iannuzzo, and F. Blaabjerg, "Wear-Out Condition Monitoring of IGBT and mosfet Power Modules in Inverter Operation," *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 6184-6192, 2019.

[70] S. Dusmez, M. Bhardwaj, L. Sun, and B. Akin, "In Situ Condition Monitor-

ing of High-Voltage Discrete Power MOSFET in Boost Converter Through Software Frequency Response Analysis," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 12, pp. 7693-7702, 2016.

[71] S. Yang, D. Xiang, A. Bryant, P. Mawby, L. Ran, and P. Tavner, "Condition Monitoring for Device Reliability in Power Electronic Converters: A Review," *IEEE Transactions on Power Electronics*, vol. 25, no. 11, pp. 2734-2752, 2010.

[72] M. Sievers, B. Findenig, M. Glavanovics, T. Aichinger, and B. Deutschmann, "Monitoring of parameter stability of SiC MOSFETs in real application tests," *Microelectronics Reliability*, vol. 114, 2020.

[73] J. O. Gonzalez, and O. Alatise, "Impact of the gate driver voltage on temperature sensitive electrical parameters for condition monitoring of SiC power MOSFETs," *Microelectronics Reliability*, vol. 76–77, pp. 470-474, 2017.

[74] Y. Peng and H. Wang, "Duty Cycle based Condition Monitoring of MOSFETs in Digitally-Controlled DC-DC Converters," in *Proc. 2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, Mar. 2020, pp. 364-369.

[75] A. Hanif, S. Roy, and F. Khan, "Detection of gate oxide and channel degradation in SiC power MOSFETs using reflectometry," in *Proc. 2017 IEEE 5th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Albuquerque, NM, USA, Oct. 2017, pp. 383-387.

[76] M. S. Nasrin and F. H. Khan, "Real time monitoring of aging process in power converters using the SSTDR generated impedance matrix," in *Proc. 2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, USA, Mar. 2013, pp. 1199-1205.

[77] B. Hu, Z. Hu, L. Ran, C. Ng, C. Jia, P. McKeever, P. J. Tavner, C. Zhang, H. Jiang, and P. A. Mawby, "Heat-Flux-Based Condition Monitoring of Multichip Power Modules Using a Two-Stage Neural Network," *IEEE Transac-*

tions on Power Electronics, vol. 36, no. 7, pp. 7489-7500, 2021.

[78] J. Zhang, X. Du, and S. Zheng, "Condition Monitoring of IGBT Module and Forced Air Cooling System Using Time Constants of Heat Sink Temperature Cooling Curve," in *Proc. 2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, 2020, pp. 2554-2558.

[79] Homepage of MEIDENSHA CORPORATION, [Online], Available: `https://www.meidensha.co.jp/index.html` (in Japanese) (Last viewed on Oct. 27, 2021).

[80] "CATENARY EYE," MEIDENSHA CORPORATION, BA523-3049 (in Japanese).

[81] E. Ugur, C. Xu, F. Yang, S. Pu, and B. Akin, "A New Complete Condition Monitoring Method for SiC Power MOSFETs," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 2, pp. 1654-1664, 2021.

[82] Z. Ni, X. Lyu, O. P. Yadav, B. N. Singh, S. Zheng, and D. Cao, "Overview of Real-Time Lifetime Prediction and Extension for SiC Power Converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 8, pp. 7765-7794, 2020.

[83] M. Tsukuda, L. Guan, K. Watanabe, H. Yamaguchi, K. Takao, and I. Omura, "V-I Curve Based Condition Monitoring System for Power Devices," in *Proc. 2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Vienna, Austria, Sep. 2020.

[84] H. Yamaguchi, M. Mukunoki, I. Omura, M. Tsukuda, L. Guan, K. Watanabe, "Characteristic monitoring system for predictive maintenance of power semiconductors," in *Proc. IEE Japan Joint Technical Meeting on Semiconductor Power Converter, Home and Consumer Appliances, and Vehicle Technology*, SPC-20-150/HCA-20-43/VT-20-39, Web, Sep. 2020 (in Japanese).

[85] S. Beczkowski, P. Ghimre, A. R. de Vega, S. M.-Nielsen, B. Rannestad, and P. Thogersen, "Online Vce measurement method for wear-out monitoring

of high power IGBT modules," in *Proc. 2013 15th European Conference on Power Electronics and Applications (EPE)*, Lille, France, Sep. 2013.

[86] S. Pu, F. Yang, B. T. Vankayalapati, E. Ugur, C. Xu, and B. Akin, "A Practical On-Board SiC MOSFET Condition Monitoring Technique for Aging Detection," *IEEE Transactions on Industry Applications*, vol. 56, no. 3, pp. 2828-2839, Mar. 2020.

[87] W. Lai, Y. Zhao, M. Chen, Y. Wang, X. Ding, S. Xu, and L. Pan, "Condition Monitoring in a Power Module Using On-State Resistance and Case Temperature," *IEEE Access*, vol. 6, pp. 67108-67117, 2018.

[88] U. Choi, F. Blaabjerg, S. Jorgensen, S. Munk-Nielsen, and B. Rannestad, "Reliability Improvement of Power Converters by Means of Condition Monitoring of IGBT Modules," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7990-7997, 2017.

[89] S. Saha, J. R. Celaya, V. Vashchenko, S. Mahiuddin, and K. F. Goebel, "Accelerated aging with electrical overstress and prognostics for power MOSFETs," in *Proc. IEEE 2011 EnergyTech*, Cleveland, OH, USA, May 2011, pp. 1-6.

[90] T. Hillebrand, S. Paul, and D. Peters-Drolshagen, "A New Approach to Threshold Voltage Measurements of Transistors," in *Proc. 2018 IEEE 24th International Symposium on On-Line Testing And Robust System Design (IOLTS)*, Platja d'Aro, Spain, Oct. 2018, pp. 207-213.

[91] X. Ye, C. Chen, Y. Wang, G. Zhai, and G. J. Vachtsevanos, "Online Condition Monitoring of Power MOSFET Gate Oxide Degradation Based on Miller Platform Voltage," *IEEE Transactions on Power Electronics*, vol. 32, no. 6, pp. 4776-4784, 2017.

[92] M. Tounsi A. Oukaour B. Tala-Ighil, H. Gualous, B. Boudart, and D. Aissani, "Characterization of high-voltage IGBT module degradations under PWM power cycling test at high ambient temperature," *Microelectronics*

Reliability, vol. 50, no. 9-11, pp. 1810-1814, 2010.

[93] S. Zhou, L. Zhou, and P. Sun, "Monitoring Potential Defects in an IGBT Module Based on Dynamic Changes of the Gate Current," *IEEE Transactions on Power Electronics*, vol. 28, no. 3, pp. 1479-1487, 2013.

[94] L. Qiao, F. Wang, J. Dyer, and Z. Zhang, "Online Junction Temperature Monitoring for SiC MOSFETs Using Turn-On Delay Time," in *Proc. 2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, 2020, pp. 1526-1531.

[95] F. Erturk, E. Ugur, J. Olson, and B. Akin, "Real-Time Aging Detection of SiC MOSFETs," *IEEE Transactions on Industry Applications*, vol. 55, no. 1, pp. 600-609, 2019.

[96] P. Wang, J. Zatarski, A. Banerjee, and J. Donnal, "Condition Monitoring of SiC MOSFETs Utilizing Gate Leakage Current," in *Proc.2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, 2020, pp. 1837-1843.

[97] B. J. Baliga, *Fundamentals of Power Semiconductor Devices, 2nd Edition.* Berlin: Springer, 2019.

[98] S. M. Sze, *Semiconductor Devices: Physics and Technology, 2nd Edition.* New York: John Wiley & Sons, Inc., 2002.

[99] "Power MOSFET Electrical Characteristics," Application Note, Toshiba Electronic Devices & Storage Corporation, 2019.

[100] "Semiconductor devices - Mechanical and climatic test methods - Part 23: High temperature operating life," *International Electrotechnical Commission*, IEC 60749-23, Edition 1.1, 2011.

[101] "Semiconductor devices - Discrete devices - Part 8: Field-effect transistors," *International Electrotechnical Commission*, IEC 60747-8, Edition 3.0, 2010.

[102] J. W. Palmour, B. Hull, D. Gajewski, L. Cheng, J. Liu, and S. T Allen, "Performance Characteristics and Applications for Second Generation SiC

Power MOSFETs ," in *Proc. the 2013 International Conference on Solid State Devices and Materials*, J-5-1, Fukuoka, Japan, Sep. 2013, pp. 948-949.

[103] T.-Y. Yew, Y.-C. Huang, M.-H. Hsieh, W. Wang, and Y.-H. Lee, "The impact of inverter-like transitions on device TDDB and ring oscillators," in *Proc. 2015 IEEE International Reliability Physics Symposium*, Monterey, CA, USA, Apr. 2015.

[104] "Guideline for Switching Reliability Evaluation Procedures for Gallium Nitride Power Conversion Devices," *Joint Electron Device Engineering Council (JEDEC)*, JEP180.01, Version 1.0, 2020.

[105] "Test Method for Continuous-Switching Evaluation of Gallium Nitride Power Conversion Devices," *Joint Electron Device Engineering Council (JEDEC)*, JEP182, Version 1.0, 2021.

[106] M. Sievers, M. Glavanovics C. Rhinow, B. Findenig, "Modular application relevant stress testing for next generation power semiconductors," in *Microelectronics Reliability*, vol. 100-101, 2019.

[107] B. Zhang, M. Ghassemi, and Y. Zhang, "Insulation Materials and Systems for Power Electronics Modules: A Review Identifying Challenges and Future Research Needs," *IEEE Transactions on Dielectrics and Electrical Insulation*, vol. 28, no. 1, pp. 290-302, 2021.

[108] M. M. Tousi and M. Ghassemi, "Electrical Insulation Design and Accurate Estimation of Temperature via an Electrothermal Model for a 10 kV SiC Power Module Packaging," in *Proc. 2020 IEEE Conference on Electrical Insulation and Dielectric Phenomena (CEIDP)*, East Rutherford, NJ, USA, Oct. 2020.

[109] Y. Miwa and T. Shimizu, "Development of iron loss measuring system for high power inductors," in *Proc. Annual Meeting of the Institute of Electrical Engineers of Japan*, Ehime, Japan, Mar. 2014, 4-072, p. 120 (in Japanese).

[110] C. Takami, K. Hirachi, and T. Mishima, "Research on All Operation Modes

of Chopper Topology Incorporating Series Connection of Buck and Boost Choppers," *Journal of the Japan Institute of Power Electronics*, vol. 37, pp. 89-96, 2012 (in Japanese).

[111] D. Yamaguchi and K. Wada, "Current Ripple Control Method of a Test System for Continuous Switching Operation of a Power Device Consisting of a Cascaded Choppers," in *Proc. IEE Japan Industry Applications Society Conference*, Nagasaki, Japan, Aug. 2019, 1-108, pp. 436-439 (in Japanese).

[112] "SiC Power Module BSM120D12P2C005 Datasheet," ROHM Co., Ltd., Kyoto, Japan, Datasheet Rev.001, Jul. 2019.

[113] H. Fujita, H. Yamashita, and H. Akagi, "Control and Performance of Digital Current-Control Schemes," *Journal of the Japan Institute of Power Electronics*, vol. 29, no. 1, pp. 93-100, 2004 (in Japanese).

[114] "Silicon Carbide Power MOSFET C2M0280120D Datasheet," Cree, Inc., North Carolina, United States, Datasheet Rev.3, Feb. 2021.

[115] "SCT2280KE Datasheet," ROHM Co., Ltd., Kyoto, Japan, Datasheet Rev.001, Mar. 2021.

[116] "SCT3160KL Datasheet," ROHM Co., Ltd., Kyoto, Japan, Datasheet Rev.005, Jun. 2018.

[117] "IMW120R220M1H CoolSiC^{TM} 1200V SiC Trench MOSFET Silicon Carbide MOSFET Datasheet," Infineon Technologies AG, Neubiberg, Germany, Datasheet Rev.2.2, Dec. 2020.

[118] D. K. Schroder, *Semiconductor Material and Device Characterization, 3rd Edition.* New York: John Wiley & Sons, Inc., 2006.

[119] E.H. Nicollian and J.R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology.* New York: Wiley, 2002.

[120] H. Tanaka, "Optimal method for C–V (capacitor–voltage) measurement," 2013 Tektronix/KEITHLEY Innovation Forum, B-5, 2013 (in Japanese).

[121] T. Sugano, T. Kato, T. Okumura, S. Komiya, M. Ozeki, and O. Ueda,

Semiconductor Evaluation Technology. Tokyo: Sangyo Tosho Publishing Co., Ltd., 1991 (in Japanese).

[122] M. Yoshizawa, K. Fukuda, K. Takasaki, N. Furuya, T. Yoshimura, and H. Nishiyama, *Practical Electrical and Electronic Measurement (Revised Edition).* Tokyo: CORONA PUBLISHING CO., LTD., 2020 (in Japanese).

[123] M. Takamiya, "Power electronics going digital for IoT/AI implementation," *The Journal of The Institute of Electrical Engineers of Japan*, vol. 141 no. 5 pp. 292-295, 2021 (in Japanese).

Journal Papers

- S.-I. Hayashi and K. Wada, "Accelerated aging test for gate oxide degradation in SiC MOSFETs for condition monitoring," *Microelectronics Reliability*, vol. 114, 113777, 6 pages, 2020.
- S.-I. Hayashi and K. Wada, "Accelerated aging for gate oxide of SiC MOSFETs under continuous switching conditions by applying advanced HTGB test," *Microelectronics Reliability*, vol. 126, 114213, 6 pages, 2021.
- S.-I. Hayashi and K. Wada, "Design a Continuous Switching Test Circuit for Power Devices to Evaluate Reliability," *IEEJ Journal of Industry Applications*, vol. 11, no. 1, pp. 108-116, 2022.
- S.-I. Hayashi and K. Wada, "Gate Drive Circuit with Input Capacitance C_{iss} Measurement Function for the Condition Monitoring of Power Devices," *IEEJ Transactions on Industry Applications*, vol. 142, no. 6, 9 pages, Accepted (in Japanese).

Article

- S.-I. Hayashi, "Conference Report: The 32nd IEEE International Symposium on Power Semiconductor Devices and ICs (ISPSD 2020) September 13-18, 2020, Virtual," *IEEJ Transactions on Industry Applications*, vol. 141, no. 3, p. NL3-2, 2021 (in Japanese).

International Conference

- S.-I. Hayashi and K. Wada, "Accelerated aging test for gate oxide degradation in SiC MOSFETs for condition monitoring," *The 31st European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2020)*, vol. 114, 113777, Athens, Greece (virtual), Oct. 2020, 6 pages.
- S.-I. Hayashi and K. Wada, "Gate Oxide TDDB Evaluation System for SiC Power Devices under Switching Operation Conditions," *The 9th International Power Electronics and Motion Control Conference (IPEMC2020-ECCE Asia)*, Nanjing, China (virtual), Nov. 2020, pp. 3525-3530.
- S.-I. Hayashi and K. Wada, "Gate-oxide degradation characteristics of SiC MOSFETs under continuous switching conditions," *The 32nd European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF 2021)*, Bordeaux, France (virtual), Oct. 2021, 6 pages.
- S.-I. Hayashi and K. Wada, "Gate Drive Circuit Having *In-Situ* Condition Monitoring System for Detecting Gate Oxide Degradation of SiC MOSFETs," *The IEEE Applied Power Electronics Conference and Exposition (APEC 2022)*, Houston, TX, USA, Mar. 2022, 8 pages, Accepted.

Domestic Conference

- S.-I. Hayashi and K. Wada, "TDDB test of MOSFETs under the switching conditions," *The 2019 IEEJ Industry Applications Society Conference*, 1-106, Nagasaki, Japan, Aug. 2019, 2 pages (in Japanese).
- S.-I. Hayashi and K. Wada, "Power regenerative continuous switching test system for power devices," *IEEJ Joint Technical Meeting on Electron Devices and Semiconductor Power Converter*, EDD-20-061/SPC-20-211, Sapporo, Japan (virtual), Dec. 2020, pp. 69-74 (in Japanese).
- S.-I. Hayashi and K. Wada, "Gate Drive Circuit with Function to Measure Input Capacitance C_{iss}–v_{GS} Characteristics for the Purpose of Condition Monitoring of Power Semiconductor Devices," *IEEJ Joint Technical Meeting on Electron Devices and Semiconductor Power Converter*, EDD-21-048/SPC-21-138, Virtual, Oct. 2021, pp. 43-48, **[Student Encouragement Award]**, (in Japanese).

Other Achievements

- S.-I. Hayashi, "Study on High Reliability of Power Conversion Circuits Based on Degradation Life Prediction by Condition Monitoring of Power Devices," 2019 Japan Power Academy Research Grant (Doctoral Student Bracket) Accepted, 2019.
- S.-I. Hayashi, "Study on High Reliability of Power Conversion Circuits Based on Degradation Life Prediction by Condition Monitoring of Power Devices," 2021 Japan Power Academy Research Grant Report Meeting, 2021, [**Award of Excellence**].

The following achievements are not related to this doctoral dissertation

- S.-I. Hayashi and K. Wada, "Design of common source inductance of MOSFET," *The 2015 Annual Meeting of the Institute of Electrical Engineering of Japan*, 4-105, Tokyo, Japan, Mar. 2015, 2 pages (in Japanese).
- S.-I. Hayashi and K. Wada, "Design for common source inductance of SiC-MOSFET," *IEEJ Joint Technical Meeting on Semiconductor Power Converter and Motor Drive*, SPC-15-140/MD-15-111, Hokkaido, Japan, Aug. 2015, 6 pages (in Japanese).
- S.-I. Hayashi and K. Wada, "Study of influence of common source inductance of MOSFET for switching operations," *The 2015 IEEJ Industry Applications Society Conference*, 1-113, Oita, Japan, Aug. 2015, 4 pages (in Japanese).
- S.-I. Hayashi, K. Wada, and Y. Suzuki, "Experimental verifications of magnetic field generator producing short-period sinusoidal waveform for *in vitro*

and *in vivo* exposure systems with high dose," *The 8th 2015 Korea-Japan Joint Conference on EMT/EMC/BE (KJJC-2015)*, P-23, Sendai, Japan, Nov. 2015, 2 pages.

- K. Wada, S.-I. Hayashi, Y. Suzuki, M. Ikehata, S. Yoshie, A. Saito, and S. Nakasono, "Design and implementation of multi-frequency magnetic field generator producing sinusoidal current waveform for biological researches," *The 18th 2016 European Conference on Power Electronics and Applications (EPE'16 ECCE Europe)*, Karlsruhe, Germany, Sep. 2016, 8 pages.
- S.-I. Hayashi and K. Wada, "Implementation of a Gate Drive Circuit for Reducing Switching Loss and Surge Voltage," *IEEJ Transactions on Industry Applications*, vol. 136, no. 10, pp. 791-797, 2016 (in Japanese).
- R. Shirai, S.-I. Hayashi, and K. Wada, "Noise Analysis Considering Equivalent Series Resistance Derving from Output Capacitance," *The 2021 IEEJ Industry Applications Society Conference*, 1-60, Nagaoka, Japan, Aug. 2021, 4 pages (in Japanese).
- K. Horii, R. Morikawa, R. Katada, K Hata, T. Sakurai, S.-I. Hayashi, K. Wada, I. Omura, M. Takamiya, "Equalization of DC Current and Surge Current in Two Parallel Connected SiC MOSFETs Using Dual Output Digital Gate Driver IC," *The 2021 IEEJ Industry Applications Society Conference*, 1-72, Nagaoka, Japan, Aug. 2021, 4 pages (in Japanese).
- S.-I. Hayashi, T. Yamamoto, S.-I. Matsumoto, and T. Takeoka, "POWER CONVERSION DEVICE," Patent, no. 6952915, 2021.
- R. Shirai, S.-I. Hayashi, and K. Wada, "Accurate MOSFET Modeling Approach with Equivalent Series Resistance of Output Capacitance for Simulating Turn-Off Oscillation," *The Applied Power Electronics Conference (APEC 2022)*, Houston, TX, USA, Mar. 2022, Accepted.
- K. Horii, R. Morikawa, R. Katada, K Hata, S.-I. Hayashi, K. Wada, I. Omura, M. Takamiya, "Equalization of DC and Surge Components of Drain

Current of Two Parallel-Connected SiC MOSFETs Using Single-Input Dual-Output Digital Gate Driver IC," *The Applied Power Electronics Conference (APEC 2022)*, Houston, TX, USA, Mar. 2022, Accepted.

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