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（LSI デバイスの信頼性のための回路レイアウト解析手法に関する研究）
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【論文の内容の要旨】

LSIs are indispensable electronic devices in the current and future society, so-called smart society, with the rapid progress of IDTs (Information and digital technologies). Especially, system on chips (SoCs) and microcontrollers (MCs) are used in cars, which realize new functions such as automatic driving, etc. MCs are used as infrastructure for protecting authentication and personal information in the new lifestyles. Those LSIs are required to have the most reliability for safety and security. In general, reliability of LSIs is quantitatively indicated by the occurrence rate of failures during long endurance tests. To demonstrate their reliability by having no record of defective products is a stringent requirement from users, which is called "zero-defect requests." However, there is a non-zero risk of failures after the product has been distributed due to defects in the manufacturing process or unseen problems in circuit design.

In the past, the efforts to make manufacturing easier by considering the impact of the layout designs on the process have been developed as design for manufacturing (DFM) using rigorous computation. However, due to the increasing integration of LSIs, it has become very difficult by simulation at realistic costs to predict processes and to specify

defects in the early stage of manufacturing. In reality, the quality of testing is becoming important in order to control the leakage of defective chips (called test-escapes). The conventional test coverage which is calculated using number of faults assumed in test vectors. However, this indicator was unrelated to layout design and therefore did not always allow to discuss the actual risk of failure.

To address these problems on LSI reliability, this dissertation focusing on failure caused by LSI layout, discusses a method for analyzing the circuit layout of LSI and evaluates a method for quantifying the risk of test escape due to layout related failure. First, an AI (artificial intelligence) technique is explored for LSI layout analysis to predict defective area in layouts. In addition, using the technique of image feature extraction, a scheme to infer the root cause of defects is discussed. And second, an indicator called physical test coverage to express realistic test quality using a technique of layout analysis called critical area analysis (CAA) is discussed and the effect of reducing test escapes is estimated.

This dissertation is organized as follows:

Chapter 1 discusses the overall content of the dissertation.

In Chapter 2 as preliminaries, the technologies related to the analysis of LSI defects are reviewed. First, in section 2-1, the conventional analysis methods for LSI defects are summarized. The purpose of physical failure analysis (PFA) is to identify, observe, and analyze the points that cause defects, and each technique is narrowed down from a relatively wide range to a narrow range. Section 2-2 describes yield models and calculation algorithms for predicting the failure rate and yield. CAA calculation method for analyzing the layout and predicting the yield is explained. Sections 2-3 summarize the issues on DFM from the design stage to improve yields and reliability. Circuit redundancy, OPC (optical proximity correction), hotspot countermeasures for lithography process-margin expansion, CMP, and CAA analysis are commonly discussed as DFM techniques. In Sections 2-4, an overview of machine learning and AI technologies, which are also the subject of this paper are given.

In Chapter 3, a method for estimating the defective locations by analyzing the layout of a certain LSI product is discussed. The defects were identified by PFA, focusing on the defects that were presumed to be caused by the layout of the product. Here, the image of

the circuit layout is cut out into squares called segments of a specific size and used as the data for analysis. A method is proposed to classify each segment with the computational model generated by learning the image data with Convolutional Neural Network (CNN), and to identify the layout which has a risk of defective occurrence. Models with 3 and 15 CNN computational layers are generated to compare the classification performance of layout images. This study verifies by cross-validation whether the computational model learned can classify layout images near actual defects as having a risk of failure. A prototype of a hazard map to identify the defective locations in the layout of an entire LSI product chip is created using the output values of the calculation model.

In Chapter 4, the feature extraction of the layout images, which is the basis of the classification performance of the circuit layout images of LSI using the CNN model in Chapter 3, is mainly studied. It is shown that the extracted features of layout images are affected by the resolution of the image data. The layout of feature points extracted from high-resolution images is investigated in detail and the features of the layouts of defective points are shown. In addition, the number of data to train the models is tried to increase to compensate for the decrease in classification performance of high-resolution images due to the limitation of the input size of the model.

Chapter 5 is a study of a method to quantify the risk of LSI test escape by applying CAA analysis using layout. Test coverage using CAA is referred to as physical test coverage, and the details of how CAA and physical coverage are calculated are described in this section. In the physical coverage analysis, wires undetected in tests are focused and the risk of test escape is estimated using the CA of undetected wires. Investigating the CA of each net and applying the test pattern to particularly long lines reduce the CA of undetected wires and test escape is effectively reduced. The conventional test coverage and physical coverage for multiple LSI products are compared. Examples of test pattern development scheme using physical coverage are estimated to effectively reduce test escapes.

Chapter 6 concludes the dissertation and summarizes the contributions of our work. The remaining issues for future study and exploration are also discussed in this chapter.