Control Strategy for Improving Efficiency of Photovoltaic System with Active Power Decoupling

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Chapter 1

Introduction

1.1 Background

1.1.1 Trends in energy and photovoltaic(PV) power generation system

There is a growing movement toward carbon neutrality, which aims to reduce greenhouse gas emissions to zero. Renewable energies are expected to replace fossil fuels as energy sources. Renewable energies such as photovoltaic, wind, geothermal, small- and medium-sized hydro-power, and biomass are promising, diverse, and essential low-carbon domestic energy sources that can contribute to energy security because they do not emit greenhouse gases and can be produced domestically. In 2021, the Sixth Strategic Energy Plan set a target of 34–36% renewable energy by 2030 [1]. Fig. 1.1 (a) shows the actual power generation in 2020, and Fig. 1.1 (b) shows the forecast for 2030 [2]. The forecast is to increase the share of renewable energy generation from 19.8% in 2020 to 36–38% by 2030. Photovoltaic power generation accounts for the largest share of renewable energy

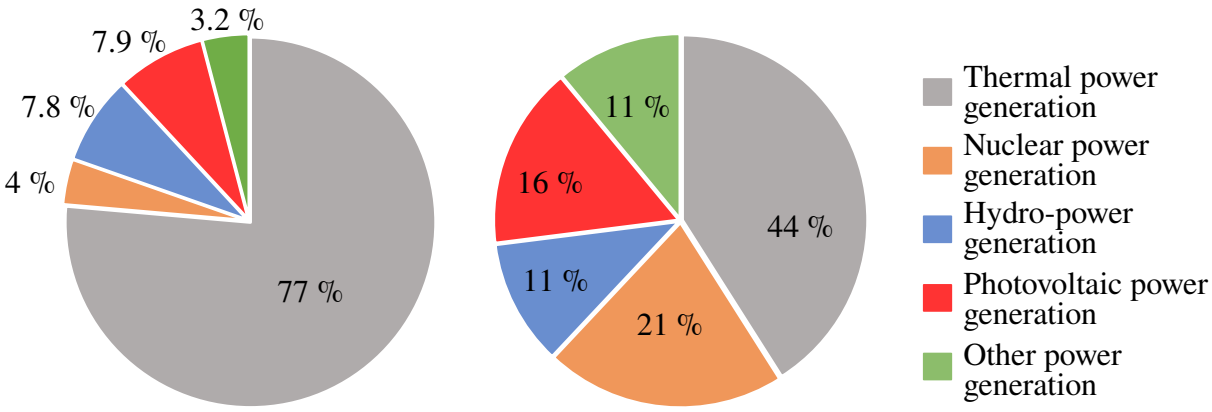


Figure 1.1. Power Supply Composition in Japan. (a) 2020. (b) 2030(Prediction).

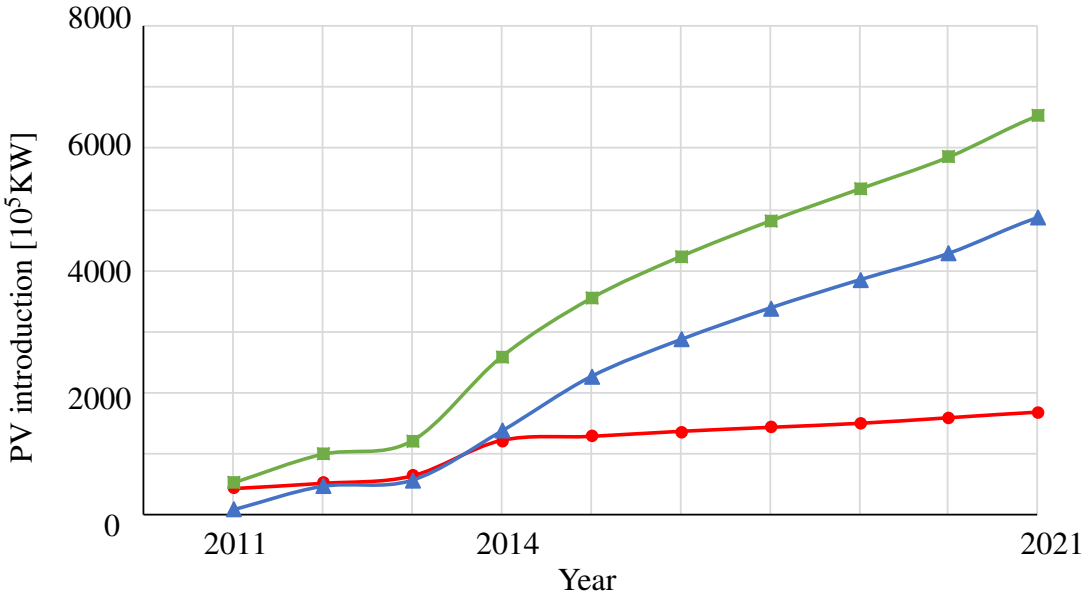


Figure 1.2. PV introduction in Japan.

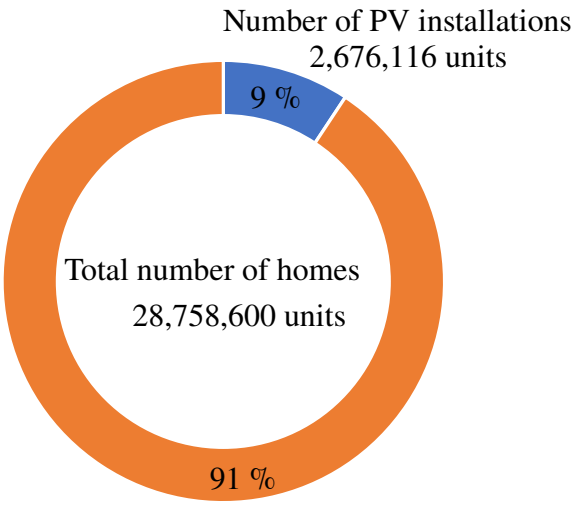


Figure 1.3. Diffusion rate of residential PV power generation system.

generation. Photovoltaic power generation is expected to be the leading method of power generation from renewable energies because "there are basically no restrictions on the area where it can be installed because the energy source is sunlight." "It can be installed on unused spaces such as roofs and walls; no new space is required.

Fig. 1.2 shows the recent domestic installed base of residential and industrial photovoltaic (PV) power generation systems in Japan [3], [4]. Since 2011, when the Great East Japan Earthquake occurred, PV systems have spread rapidly, and the total number of PV systems installed in 2021 will be approximately 13 times greater than that in 2011. On

the other hand, focusing only on residential PV systems, the increase in the number of PV systems installed has been limited to approximately 4 times, and the amount of PV systems installed each year is also on a decreasing trend. Fig. 1.3 shows the diffusion rate of residential PV systems [5]. The number of residential PV systems installed is still 9% of the total number of homes, indicating that there is room for growth in the market.

The Ministry of Economy, Trade, and Industry (METI), the Ministry of the Environment (MOE), and the Ministry of Land, Infrastructure, Transport and Tourism (MLIT) are working together to promote the construction of self-consumption houses called zero energy houses (ZEH) [6]. ZEH refers to "buildings and houses that aim to achieve net-zero annual primary energy consumption from renewable energy sources such as photovoltaic power generation while saving energy.

1. Buliding airtight houses with insulation performance higher than the standard value.
2. Introducing high-efficiency and high-performance energy-saving lighting, ventilation, hot water supply, air-conditioning, etc.
3. Introducing a power generation system capable of compensating 100% of primary energy consumption.

Residential PV systems are expected to serve as the power generation system for this ZEH. In addition, the Sixth Energy Plan states that the government's goal is "to ensure energy-saving performance at the level of the ZEH standard for new houses built after 2030" and "to have PV systems installed in 60% of new detached houses by 2030," and subsidies are being provided for this purpose. Therefore, the demand for residential PV systems in newly built houses is expected to increase.

One of the factors contributing to the high installed capacity of industrial PV systems, which are large capacity systems, is the lower cost of power generation compared to residential PV systems. Fig. 1.4 shows the generation costs of residential and industrial PV systems in 2013 and 2020 [7–9]. Generation cost is defined by 1.1:

$$\text{Generation\_cost}[\text{yen/kWh}] = \frac{\text{Capital\_cost} + \text{Operation\_and\_maintenancecost}}{\text{Operating\_years} \times \text{Annual\_power\_generation}} \quad (1.1)$$

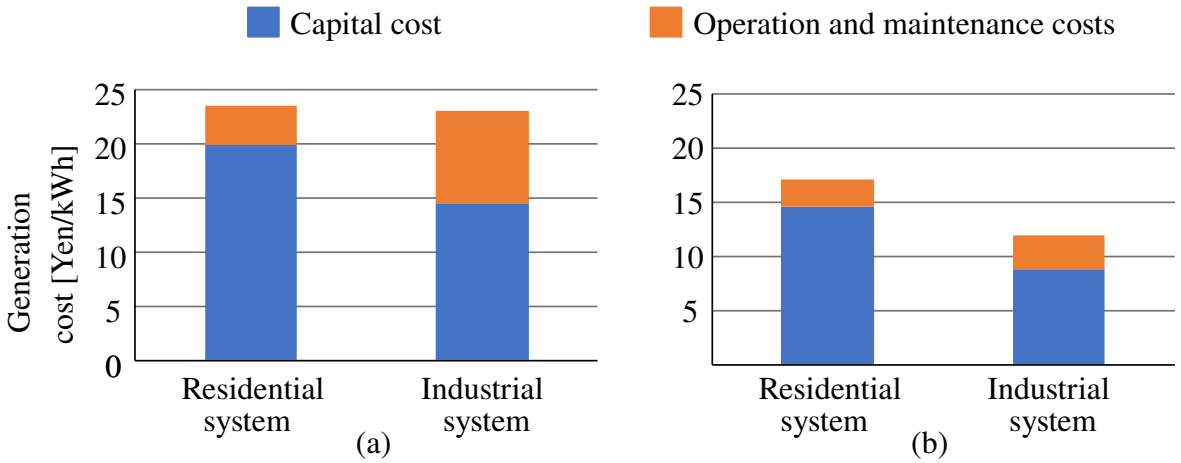


Figure 1.4. Power generation cost of PV system. (a) 2013. (b) 2020.

the capital cost, including initial cost and disposal cost of the system and operation and maintenance cost, divided by total power generation derived from the number of years of operation and annual power generation. Fig. 1.4(a) shows that there is no significant difference in power generation costs between industrial and residential PV systems in 2013, when there is no significant difference in the number of PV systems installed. On the other hand, in 2020, the generation cost for industrial use is 17.1 yen/kWh for residential systems and 12.0 yen/KWh for industrial systems. Comparing residential and industrial PV systems over the same number of years of operation, the difference in power generation and system cost shows that the cost of industrial PV systems, which are built on a larger scale, tend to be lower. Furthermore, industrial PV systems do not need to consider the area of the photovoltaic array (PV array) or the effects of the surrounding environment. In contrast, residential PV systems need to be installed in a limited space on the roof, considering the shading effects of surrounding buildings, making it difficult to construct a large-capacity system. It is necessary to have a high system power generation efficiency and larger amount of power generated through long-term operation to reduce the cost of power generation for residential PV systems.

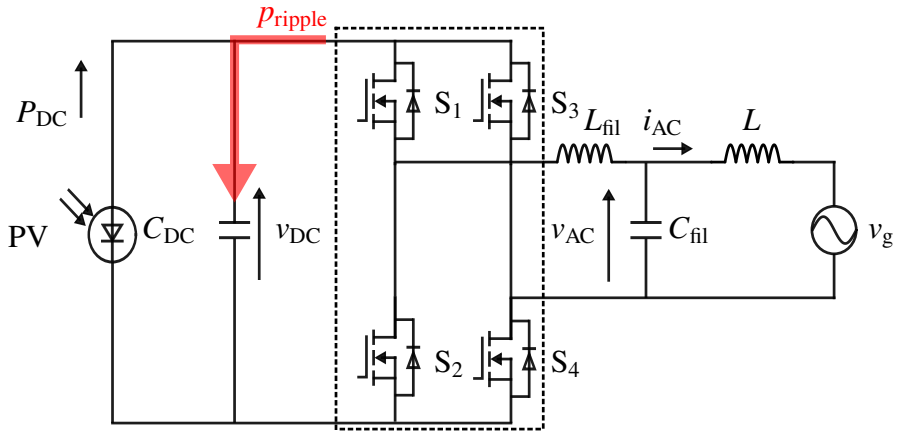


Figure 1.5. Residential PV power generation system.

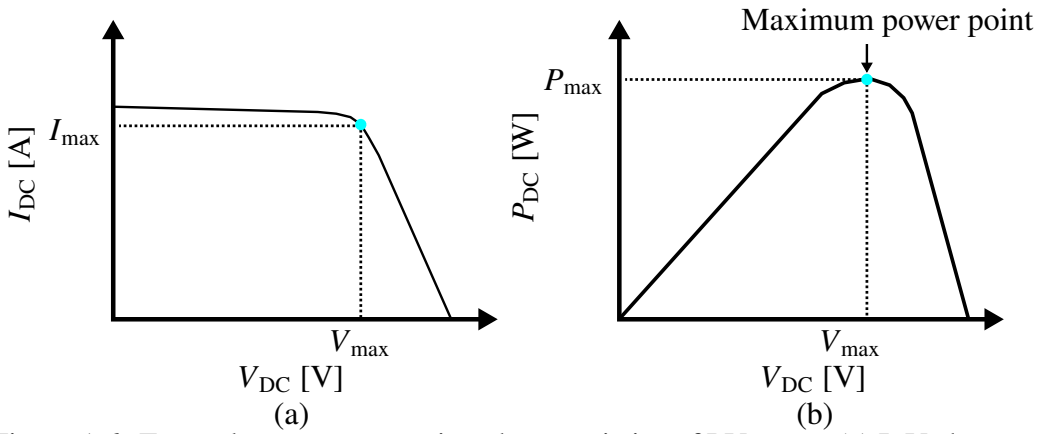


Figure 1.6. Example power generation characteristics of PV array. (a) I–V characteristics. (b) P–V characteristics.

1.1.2 Extended life-time of a PV system

Fig. 1.5 shows the configuration of a PV system. PV array generates DC power and converts it to AC power corresponding to the distribution system using a grid-connected inverter, which is a power conversion circuit. Fig. 1.6 shows an example of the power generation characteristics of a PV array. PV array outputs a DC current I_{DC} in response to an applied DC voltage V_{DC}. The system power generation efficiency of a PV system η_{system} is obtained from the power generation efficiency of the PV array η_{PV} and the power conversion efficiency of PCS $\eta_{circuit}$, as shown in (1.2).

$$\eta_{system} = \frac{\eta_{PV}\eta_{circuit}}{100}[\%] \tag{1.2}$$

Eq. (1.3) shows the PV generation efficiency η_{PV}, which is derived from the DC power P_{DC} generated by the PV array relative to the maximum potential power of the PV array P_{max}.

$$\eta_{\mathrm{PV}} = \frac{P_{\mathrm{DC}}}{P_{\mathrm{max}}} \tag{1.3}$$

The power conversion efficiency η_{circuit} is expressed as the ratio of the output AC power p_{AC} to the DC power P_{DC}, as expressed in (1.4).

$$\eta_{\mathrm{circuit}} = \frac{p_{\mathrm{AC}}}{P_{\mathrm{DC}}} \tag{1.4}$$

The PV array outputs its maximum power when the inverter controls the DC voltage according to the characteristics of the PV array.

The inverter has the characteristic of converting DC power P_{DC} to AC power p_{AC}, which causes power pulsations to propagate on the DC side. The AC power is expressed by (1.5).

$$\begin{aligned} p_{\mathrm{AC}} &= i_{\mathrm{AC}} \times v_{\mathrm{AC}} = \sqrt{2} I_1 \sin\omega_{\mathrm{g}} t \times \sqrt{2} V_1 \sin\omega_{\mathrm{g}} t \\ &= I_1 V_1 - I_1 V_1 \cos 2\omega_{\mathrm{g}} t = P_{\mathrm{DC}} - P_{\mathrm{ripple}} \cos 2\omega_{\mathrm{g}} t = P_{\mathrm{DC}} + p_{\mathrm{ripple}} \end{aligned} \tag{1.5}$$

where, v_{AC} is the output voltage, i_{AC} is the output current, V_{AC} is the RMS value of output voltage, I_{AC} is the RMS value of output current, P_{ripple} is the amplitude of p_{ripple}, and $\omega_{\mathrm{g}} t$ is the grid phase. The p_{AC} is composed of P_{DC} and power pulsation p_{ripple}.

The p_{ripple} propagates to the DC side and is absorbed by the DC capacitor C_{DC}, resulting in voltage ripple $\Delta v_{\mathrm{DCrip}}$. The voltage ripple is expressed by (1.6).

$$\Delta v_{\mathrm{DCrip2}} = \frac{P_{\mathrm{ripple}}}{\omega_{\mathrm{g}} V_{\mathrm{DC}} C_{\mathrm{DC}}} \tag{1.6}$$

Here, V_{DC} is the average DC voltage. If large DC voltage ripple exists, the PV array cannot generate power at the maximum power point and cannot output maximum power. Fig. 1.7 shows the operating waveforms at P_{max}=1 kW, v_{AC}=100 $\mathrm{V_{rms}}$, and C_{DC}=50 µF.

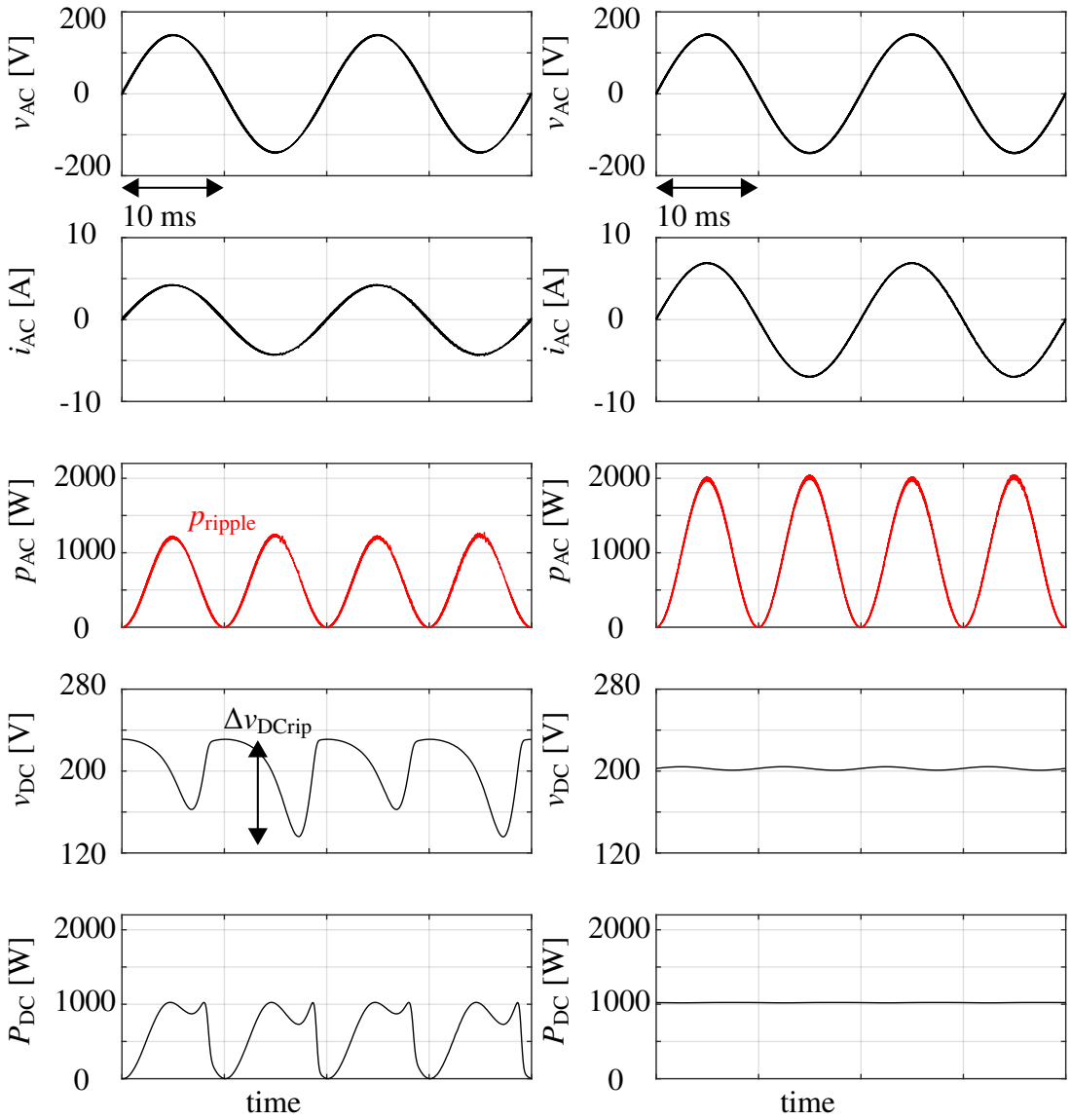


Figure 1.7. Operation waveforms with C_{DC}=50 µF

Figure 1.8. Operation waveforms with C_{DC}=4700 µF

The excessive voltage ripple is caused by insufficient capacitance. The voltage ripple also causes fluctuations in the generated power P_{DC}, leading to a decrease in the average generated power. Therefore, an inverter is required to have a power decoupling feature to absorb the pulsating power p_{ripple}.

Conventional PV systems use a passive power decoupling (PPD) method with large capacitance. Fig. 1.8 shows the operating waveforms at P_{max}=1 kW, v_{AC}=100 V_{rms}, and C_{DC}=4700 µF. The voltage ripple is suppressed and maximum power is produced by

Table 1.1. Capacitor characteristics

	Volume	Lifetime
Electrolytic capacitor	○	110,000 hour (13 years)
Film capacitor	×	200,000 hour (23 years)

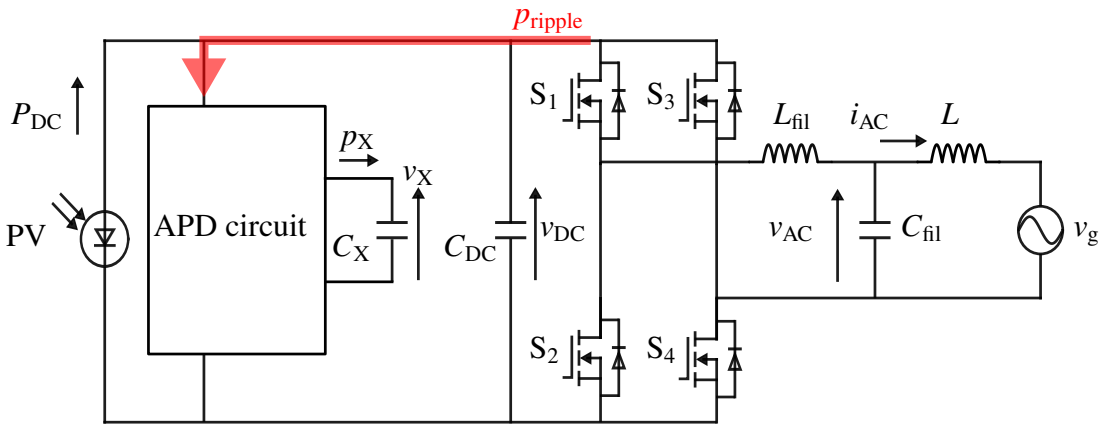


Figure 1.9. Active power decoupling method.

increasing the DC capacitance. Table 1.1 shows the different capacitor types and their characteristics [10–13]. The electrolytic capacitors are used from the viewpoint of volume since the PPD method requires a large capacitor. However, electrolytic capacitors have been reported to have a shorter life-time than film capacitors, presenting a subject for extending the lifetime of PV systems. Long-life film capacitors should be applied to PV systems for achieving voltage ripple suppression with small capacitance.

1.1.3 Active power decoupling method

Many studies have proposed an active power decoupling (APD) method to extend the lifetime of a PV system [14–35]. The APD method uses film capacitors and suppresses the DC voltage ripple to extend the lifetime of the PV system. An Inverter with APD feature consists of a single-phase inverter and an APD circuit. Many circuit types have been proposed for the APD circuit, including a buck converter type [14], [15], boost converter type [16], [17], buck-boost converter type [18], fly-back converter type [19], [20], flying capacitor converter type [21], and isolated converter type [22], [23].

Fig. 1.9 shows an example of an inverter with an APD circuit. The APD circuit charges

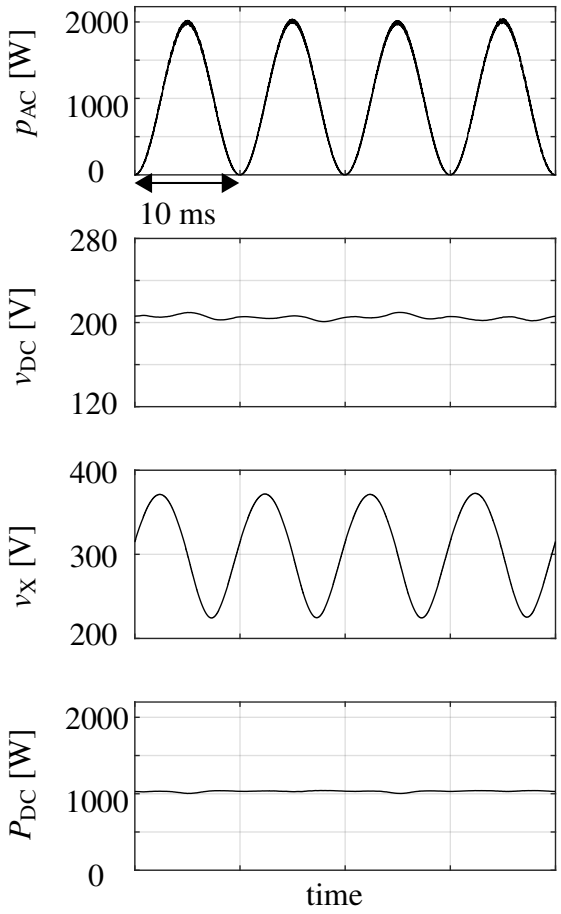


Figure 1.10. Operation waveforms with APD method.

and discharges the power pulsation p_{ripple} to the decoupling capacitor C_X to suppress the power pulsation absorbed by the DC capacitor. Fig. 1.10 shows the operating waveform with APD method at P_{max}=1 kW, v_{AC}=100 V_{rms}, C_{DC}=50 µF, and C_X=50 µF. The APD method enables the suppression of DC voltage ripple with a small capacitance compared to the PPD method. In addition, the voltage ripple of the decoupling capacitor voltage v_X does not affect the DC voltage; hence, a smaller capacitance can be used for C_X.

1.1.4 Issues in the APD Method

The APD method is known to lower the overall system efficiency owing to power conversion loss caused by additional circuits. While many conventional APD methods have focused on circuit methods to improve efficiency, more work needs to be done on control methods to improve efficiency. Fig. 1.11 shows the verification circuit configuration of

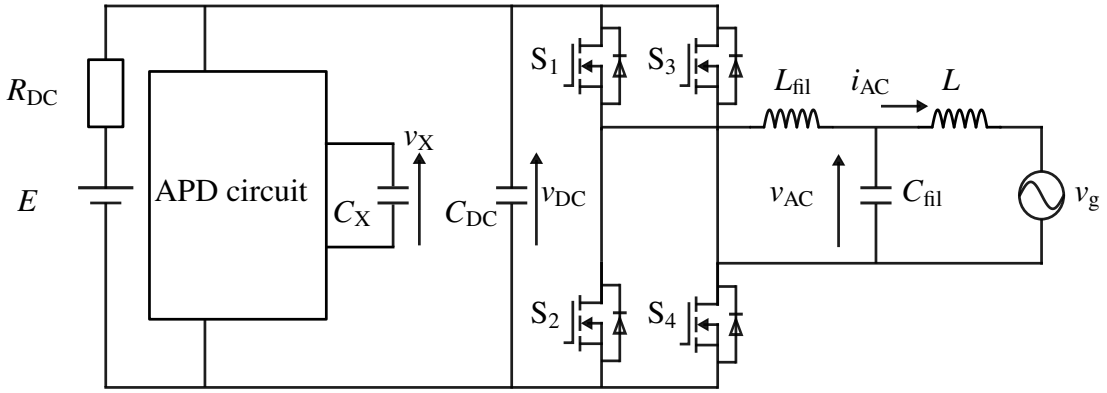


Figure 1.11. Active power decoupling method for verification.

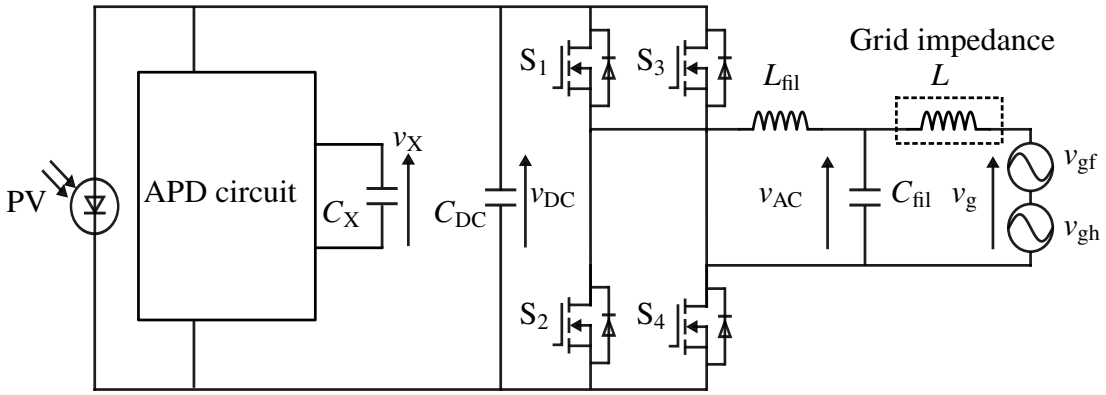


Figure 1.12. Active power decoupling method for real system.

the conventional APD method. In conventional APD methods, since the main objective is to verify the circuit method, the PV array is replaced with a simulated power supply, and the grid is replaced with an ideal power supply that does not contain harmonics in a simplified study. Fig. 1.12 shows the circuit configuration of the APD method for a real system. In a real PV system, there are factors related to APD control, such as PV power generation characteristics, grid harmonic voltage, and grid impedance. However, the system configurations in the conventional APD method can't verify the effects of the power generation characteristics of the actual PV arrays and the grid on the circuit and control operation. Therefore, it is necessary to increase the efficiency of a PV system by considering PV array and distribution grid.

1.2 Objective of this dissertation

This study develops a control strategy for inverter and APD circuits to improve the efficiency of PV power generation systems with active power decoupling features. In this dissertation, the control scheme is developed from two viewpoints: the PV array and distribution grid. For the PV array, control schemes are proposed to increase efficiency by focusing on power generation characteristics. For the distribution grid, the APD control considering harmonic voltages and grid impedance estimation with resonant characteristics are studied. This study is focused on the development of APD control, focusing on the generation characteristics of PV arrays and the effects of the distribution grid, and is unique in that it promotes the improvement of the overall system efficiency.

1.3 Dissertation structure

This dissertation consists of 7 chapters. Fig. 1.13 shows the structure of this dissertation. Chapters 1 and 2 present a summary of the research background and issues related to the APD method. Chapters 3 and 4 develop the circuits and control schemes that focus on “voltage ripple” and “partial shade,” which affect the power generation efficiency of PV arrays, to achieve higher efficiency in PV systems. Chapters 5 and 6 promote the realization of high-efficiency APD schemes by developing control schemes that focus on “grid harmonics” and “grid impedance,” which affect the voltage ripple control of APD circuits.

Chapter 1 provides a research background and describes the issues of active power decoupling schemes to achieve a long lifetime for PV systems. The need to comprehensively consider the impact of the PV array’s power generation characteristics and distribution grid on APD control, in addition to the inverter, is presented.

. Chapter 2 reviews related research and clarify issues that require solutions. While conventional studies on improving the efficiency of APD methods have mainly focused on circuit schemes, this dissertation focuses on APD control methods that consider the power generation characteristics of PV arrays. This chapter also contain a review of related studies

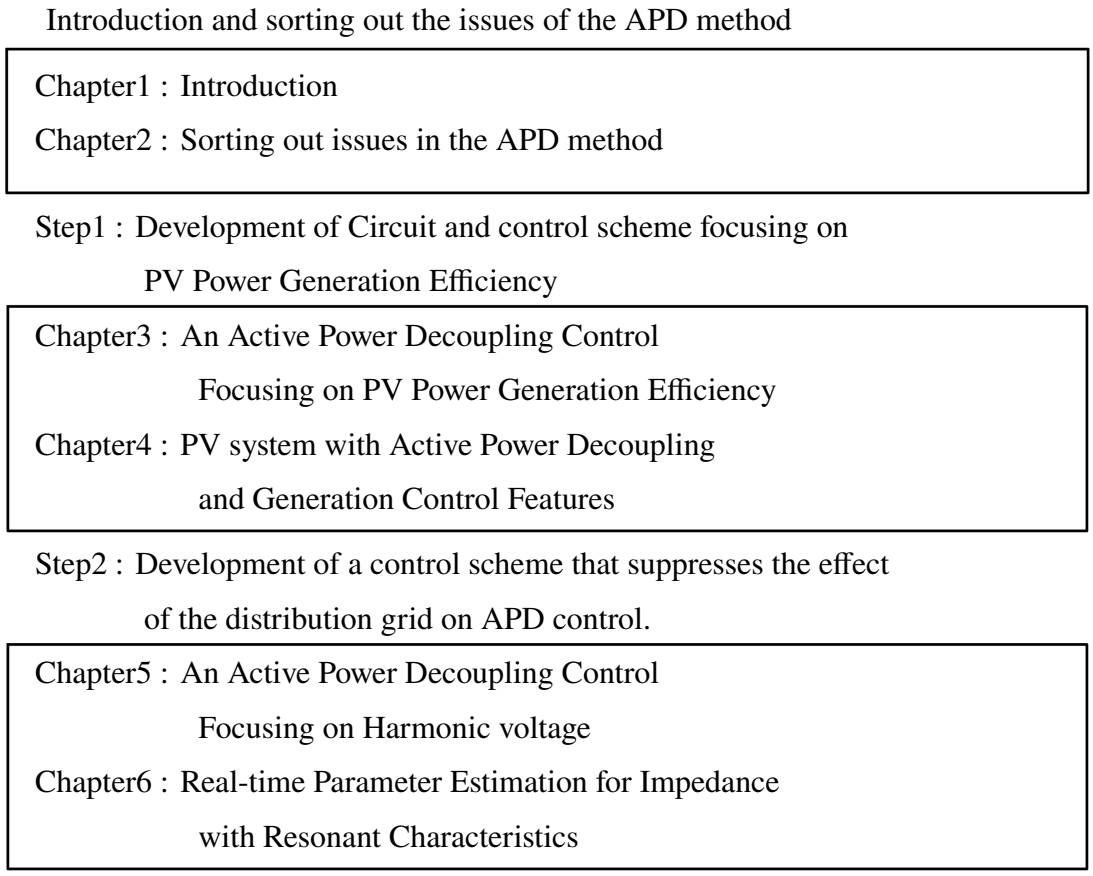


Figure 1.13. Structure of the dissertation.

on suppression techniques of partial shade and determine the partial shade suppression circuit. The impact of grid harmonics and impedance on APD control will be analyzed and evaluated mathematically. This chapter also reviews related studies on grid impedance estimation and determine the target grid impedance with resonant characteristics.

Chapter 3 describes the APD control considering the power generation characteristics of a PV array. The APD control that achieves compensated power control according to the power generated by the PV is proposed. The capacitance of the DC capacitor of a 1 kW rated inverter is derived from two design methods: a design that focuses on the voltage ripple caused by the switching frequency and a design that can maintain the allowable ripple ratio when the APD circuit is stopped at one-third of the rated operating power of 333 W or less. Real-time simulation and experimental results for an inverter with a rating

of 1 kW will clarify the difference and usefulness of the pulsation compensation of the APD circuit according to the design method of the DC capacitance.

Chapter 4 describes the circuit configuration integrating the generation control circuit (GCC) and APD method. Two circuit configurations of a PV system with both features are compared; the circuit and control characteristics of both configurations are clarified based on analysis using the state-space averaging method. In addition, a suitable configuration for the PV system is suggested from a comparison of the two circuit configurations.

Chapter 5 describes the control strategies of APD for the compensation of power pulsation caused by both fundamental and harmonic components. Furthermore, the compensating power of the APD control is discussed when the grid voltage has the 3rd harmonic voltage. The influence of the 3rd harmonic voltage on the DC voltage ripple is evaluated. In APD control, the power pulsation caused by the harmonic components is considered in the compensating power calculation. The compensating power, including the power pulsation caused by the fundamental and harmonic components, is discussed based on the DC voltage ripple. The validity of the APD control is verified on a 400 W inverter.

Chapter 6 describes estimated frequency injection and LCR parameters estimation methods for real-time estimation of grid impedance with resonant characteristics. The estimated frequency injection method focusing on impedance resonant characteristics is proposed. In addition, LCR parameters and quality factor estimation methods are proposed based on the analysis focusing on resonant characteristics for the grid impedance model.

Chapter 7 summarizes this study and discusses future works.

Chapter 2

Sorting out issues in the APD method

2.1 Voltage ripple control of APD method and power generation efficiency of PV array

2.1.1 Operation principle of APD method

The APD method has been proposed in numerous circuit schemes. Fig. 2.1 and Fig. 2.2 show example circuit configurations of the APD method.

Eq. (2.1) and Fig. 2.3 show the relationship between the inverter output power p_{AC} and DC power P_{DC}.

$$p_{AC} = i_{AC} \times v_{AC} = \sqrt{2} I_1 \sin\omega_g t \times \sqrt{2} V_1 \sin\omega_g t = I_1 V_1 - I_1 V_1 \cos 2\omega_g t = P_{DC} + p_f \quad (2.1)$$

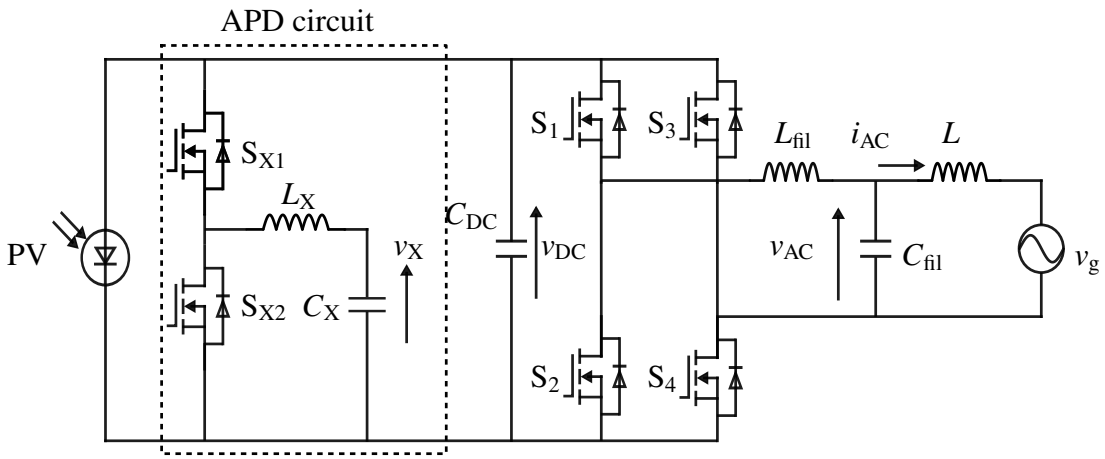


Figure 2.1. Buck type APD circuit.

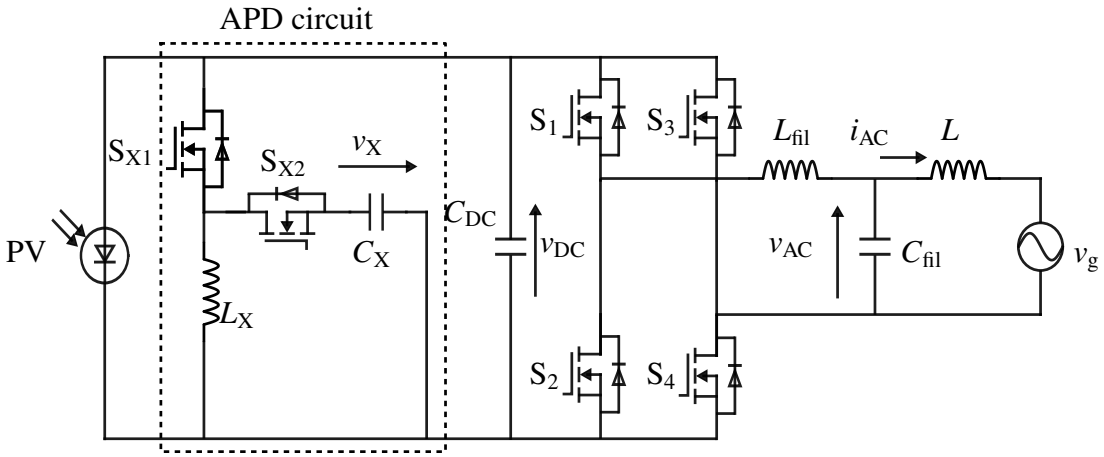


Figure 2.2. Buck-boost type APD circuit.

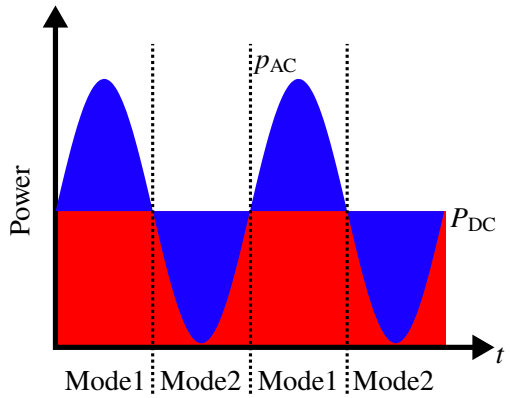


Figure 2.3. Operation principle of APD function.

where, v_{AC} is the output voltage, i_{AC} is the output current, V_{AC} is the RMS value of output voltage, I_{AC} is the RMS value of output current, and $\omega_g t$ is the grid phase. From (2.1), p_{AC} is composed of P_{DC} and power pulsation p_f. The p_{ripple} propagates to the DC side of the inverter.

The APD circuit charges and discharges the p_f propagating on the DC input side to C_X by switching the discharge mode (Mode 1) and charge mode (Mode 2) of switches S_{X1} and S_{X2} according to the relation between p_{AC} and P_{DC}. In Mode 1, the operation of S_{X2} supplies p_f from C_X to L_X and the operation of S_{X1} discharges p_f to the grid side. In Mode 2, the operation of S_{X1} supplies p_f to L_X and the operation of S_{X2} charges p_f from L_X to C_X. Because the voltage ripple of the decoupling capacitor voltage v_X does not propagate to the inverter input voltage v_{DC}, the amount of voltage ripple with the charging

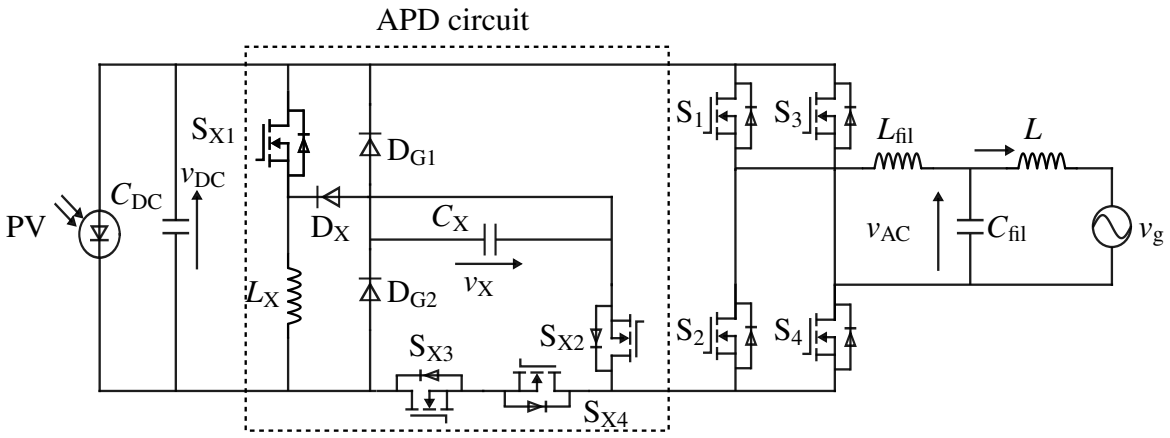


Figure 2.4. Inverter with buck-boost type APD circuit.

and discharging of C_X can be large, allowing the accumulation of necessary p_f even with a small capacitance. As a result, the use of film capacitors for C_{DC} and C_X can extend the service life of the system.

2.1.2 Circuit method for improving the efficiency of conventional APD control

Many studies have been conducted to improve the power conversion efficiency of inverters with APD feature [36–39]. Fig. 2.4 shows the configuration of the APD circuit proposed in r [36]. Ref. [36] proposes an inverter with an APD circuit consisting of a buck-boost converter and an additional diode. In the discharge operation of the decoupling capacitor C_X, the discharge path through the diode discharges the power pulsation without the decoupling inductor L_X, thereby achieving high inverter efficiency. Fig. 2.5 shows the configuration of the APD circuit proposed in [37]. Ref. [37] proposes a circuit scheme in which the boost converter of the inverter and the inductor of the APD circuit are shared. The loss and volume of the inductor are reduced, thereby achieving a smaller and more efficient power inverter.

Improving the efficiency of APD circuits has focused on the circuit scheme. On the other hand, there needs to be more studies on voltage ripple suppression targets based on the impact of voltage ripple on the power generation efficiency of PV arrays in the APD method. In this APD method, the compensating power is always maximized, which

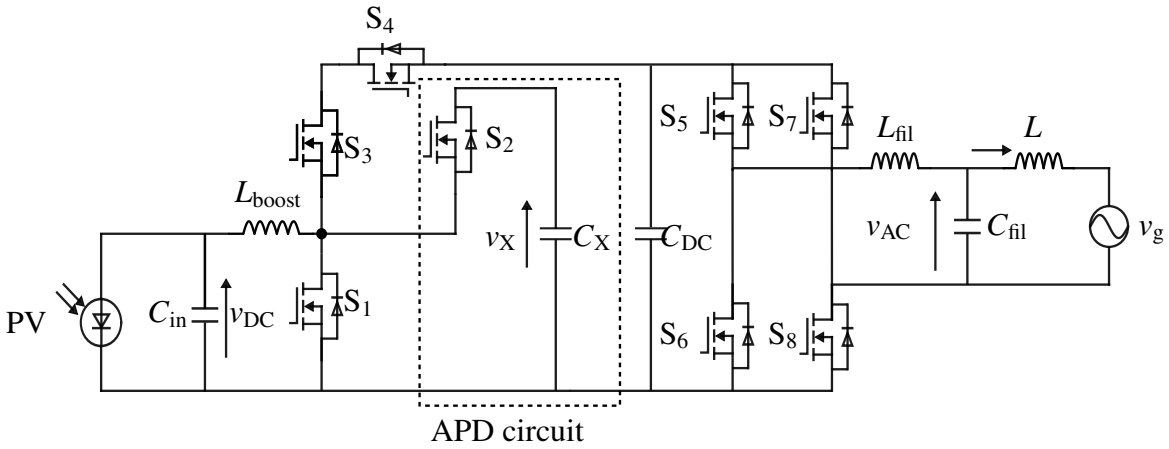


Figure 2.5. Inverter with boost type APD circuit.

leads to a decrease in system efficiency due to excessive compensation at low loads. In the conventional APD method, the voltage ripple of the PV array is always set to zero to maximize the power generation efficiency of the PV array. However, at low loads, the suppression of voltage ripple by the inverter input capacitor is sufficient to maximize the power generation efficiency of the PV array. Therefore, the system efficiency can be improved by reducing the compensating power of the APD circuit or stopping the operation of the APD circuit when the PV is under low load, thereby suppressing the power loss of the APD circuit.

2.1.3 Generation characteristics of PV array and effect of DC voltage ripple

The allowable ripple ratio is defined from the analysis using the equivalent circuit of the PV array. Here, the allowable ripple rate is the DC voltage ripple that satisfies the PV array's power generation efficiency. The PV array has characteristic of producing a current corresponding to the applied voltage v_{DC}, and this PV characteristic is represented by the equivalent circuit shown in Fig. 2.6 [40–43]. Eq. (2.2) represents the output current I_{DC} of the PV array.

$$\begin{aligned} I_{\mathrm{DC}} &= I_{\mathrm{SC}} - I_{\mathrm{d}} - I_{\mathrm{sh}} \\ &= I_{\mathrm{SC}} - I_{\mathrm{s}}\{\exp(\frac{\mathrm{e}v_{\mathrm{DC}}}{\mathrm{n}k_{\mathrm{b}}T}) - 1\} - \frac{v_{\mathrm{DC}}}{R_{\mathrm{sh}}} \end{aligned} \tag{2.2}$$

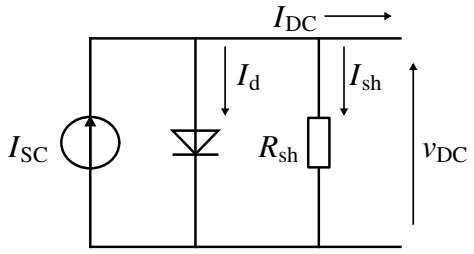


Figure 2.6. PV equivalent circuit.

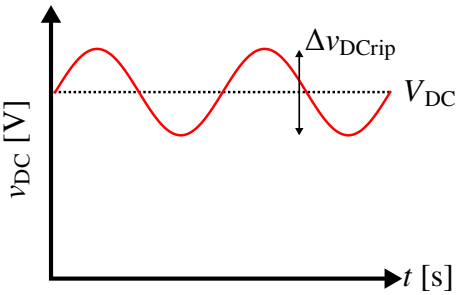


Figure 2.7. Example voltage ripple.

Table 2.1. PV parameters.

Parameter	Value
Optimal voltage V_{max}	196.6 V
Optimal current I_{max}	5.07 A
Maximum Power P_{max}	996.5 W
Short circuit current I_{SC}	5.5 A
Open circuit voltage V_{OC}	239.4 V
Diode saturation current I_s	3.62×10^{-5} A
Parallel resistor R_{sh}	1000 Ω
Elementary charge e	1.6022×10^{-19} C
Boltzmann constant k_b	1.381×10^{-23} J/K
Diode ideal coefficient n	2
Ambient temperature T	320 K

where I_{SC} is the short circuit current, I_s is the diode saturation current, e is the elementary charge, V_{DC} is the applied voltage, n is the diode ideal coefficient, k_b is Boltzmann's constant, T is the ambient temperature, and R_{sh} is the parallel resistance.

Fig. 2.7 shows an example of a voltage with ripple component of double the frequency of the grid with respect to the optimum voltage, and Table 2.1 lists the parameters of the PV array. The PV generation efficiency η_{PV} is defined by (2.3).

$$\eta_{PV} = \frac{P_{PV}}{P_{max}} \times 100 = \frac{I_{PV} v_{DC}}{I_{max} V_{max}} \times 100 \tag{2.3}$$

Where P_{max} is the maximum generation power. The voltage ripple ratio α_{VDCrip} is defined

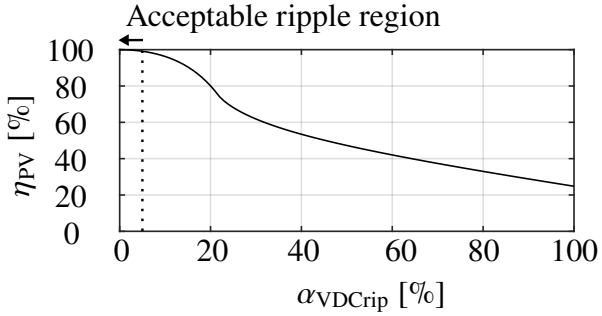


Figure 2.8. Evaluation of PV generation efficiency η_{PV}.

by equation (2.4).

$$\alpha_{VDCrip} = \frac{\Delta v_{DCrip}}{2V_{max}} \times 100 \tag{2.4}$$

where V_{max} is the optimum voltage, and $\Delta v_{rip,\,100}$ is the ripple component at 100 Hz. I_{PV} is derived by substituting the voltage of α_{VDCrip}=0–100% for the voltage V_{DC} in (2.2). The PV generation efficiency with respect to changes in the voltage ripple ratio is evaluated using (2.3).

Fig. 2.8 shows the evaluation results of the PV generation efficiency. Fig. 2.8 shows that the PV generation efficiency drops by 10% when α_{VDCrip} exceeds 15%. For α_{VDCrip} up to 5%, the reduction in PV generation efficiency is within 1% and the PV generation efficiency can be maximized. α_{VDCrip}=5% is defined as the allowable ripple ratio. During APD control, the DC voltage V_{DC} is controlled by the compensating power P_X that operates at α_{VDCrip}=5%.

2.2 Effect and suppression method of partial shade

2.2.1 Effect of partial shade on PV generation characteristics

Partial shading of a PV array (hereafter referred to as partial shade) causes a reduction in power production greater than the shaded area [44–47]. A PV array consists of multiple PV modules connected in series and parallel. The amount of power generated by each PV module is determined by the amount of solar radiation; if the PV array has partial shade, there will be a difference in the amount of power generated between the PV modules

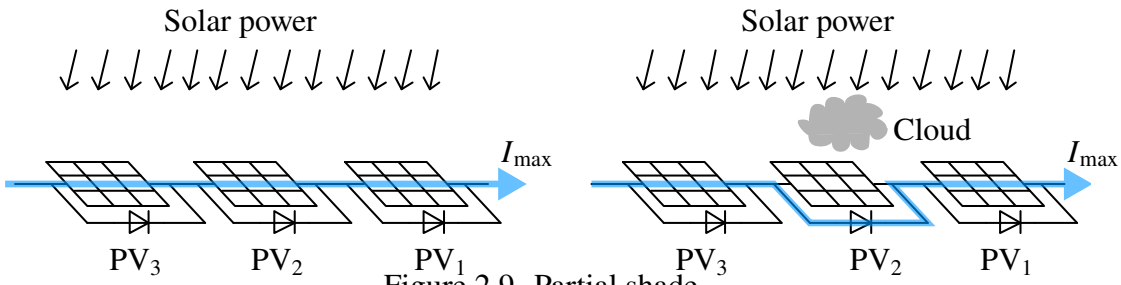


Figure 2.9. Partial shade.

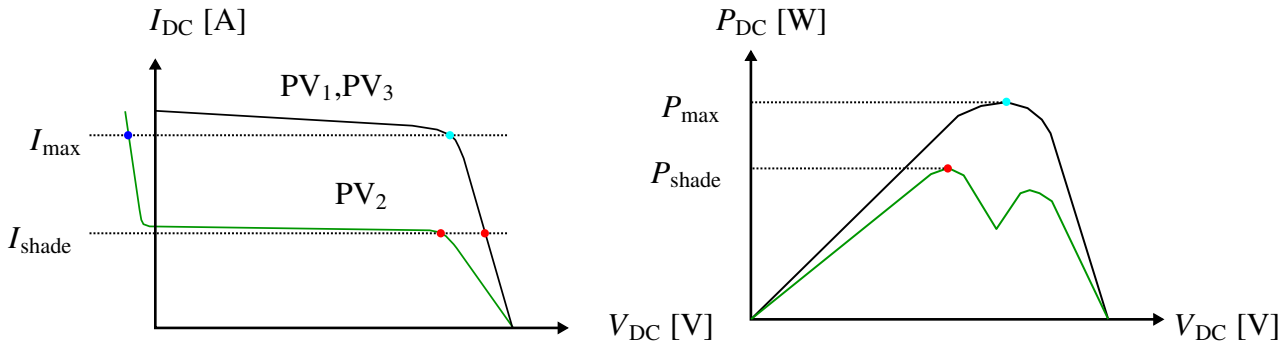


Figure 2.10. PV characteristics under partial shade condition.

depending on whether they are shaded or not. In this case, the power generation of modules other than the module whose power generation is reduced due to partial shade will also be reduced. Ref. [46] evaluates the effect of partial shading on PV power generation efficiency, noting a 37% reduction in power generation efficiency depending on the state of partial shade. Fig. 2.9 shows a bypass diode system used in conventional PV arrays, in which a diode is connected to each PV module. The diodes form a current bypass path when there is unbalanced power generation between PV modules, thereby suppressing the effects of partial shade. However, because this method bypasses the entire PV module whose power generation has declined, the power generated by the PV cells with the remaining power generation capacity cannot be extracted. Furthermore, as shown in Fig. 2.10, the P–V characteristics of the PV array with partial shading have multiple power peak points, preventing the maximum power point from being tracked by maximum power point tracking (MPPT) control.

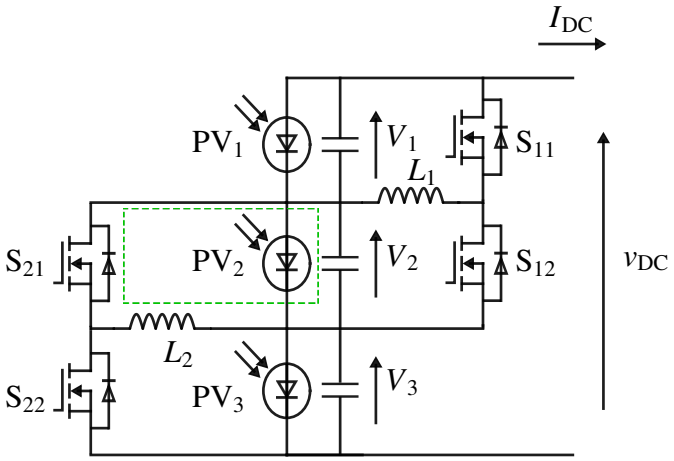


Figure 2.11. Generation control circuit.

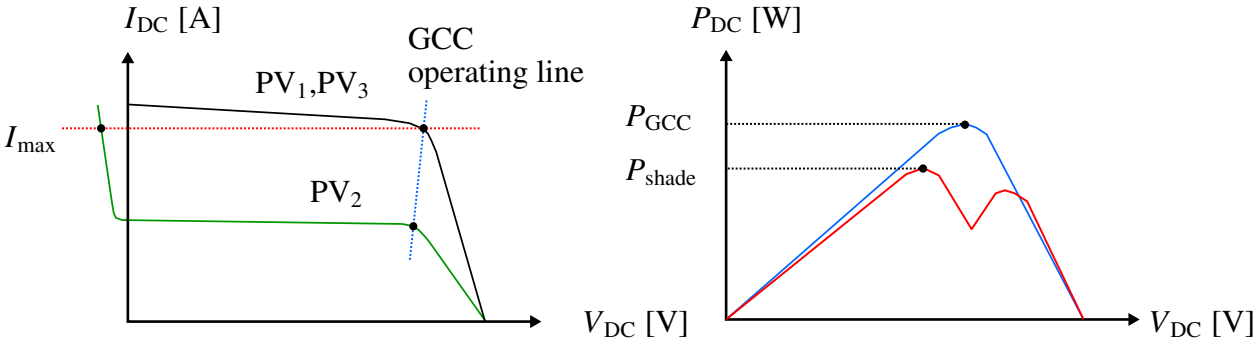


Figure 2.12. PV characteristics with GCC.

2.2.2 Generation control circuit

A partial shade suppression technique using a power conversion circuit has been proposed [48–61]. Many circuit types have been proposed for partial shade suppression, including a buck-boost converter type [48–55], switched capacitor converter type [56], [57] fly-back converter type [59]. The partial shade suppression circuit outputs the maximum power of each PV module by sending compensating power to the PV module that generates the least amount of power.

The generation control circuit (GCC) is an example of a partial shade suppression method using a power conversion circuit [48], [49]. Fig. 2.11 shows the circuit configuration of a GCC, in which buck-boost converters are connected to series-connected PV modules. This circuit is characterized by its capability to produce the maximum power output from each PV module, even in partial shade, while maintaining the series structure

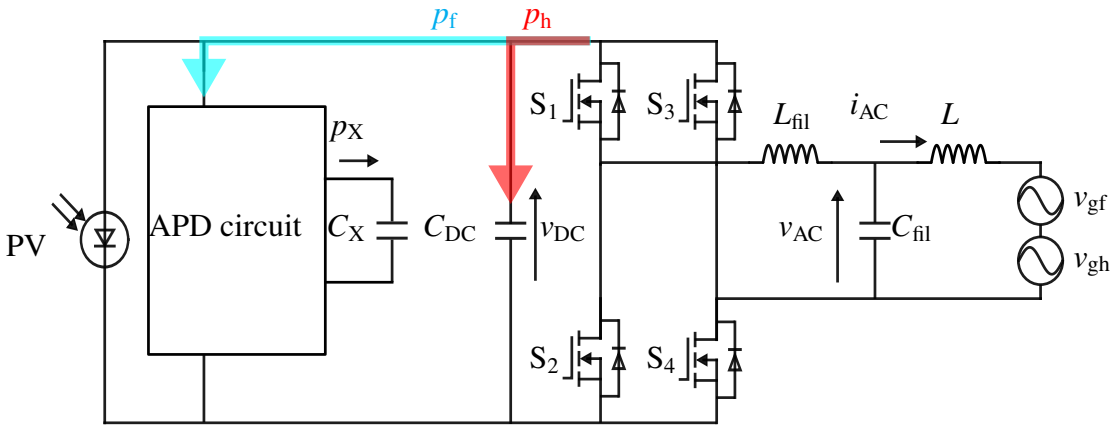


Figure 2.13. APD circuit with harmonic voltage v_{gh}.

of the PV modules. In the bypass diode method, the operating point is determined by the current, as shown in Fig 2.12 (a). Whereas in GCC, the module voltage V_1–V_3 are individually controlled to maximize the power production of each PV module by adjusting the duty ratio of each switch. As a result, the power generation characteristics of the entire PV module have a single power peak point, as shown in Fig. 2.12(b), and can produce higher generation power than the bypass diode method.

The conventional APD method does not consider the effects of partial shade. Therefore, a PV system that integrates the GCC and APD methods is proposed to develop a highly efficient and long lifetime system.

2.3 Grid harmonic voltage

2.3.1 Effect of grid harmonic voltage on APD control

The power distribution grid has grid harmonics, and studies on grid-connected inverters have proposed methods to suppress the effects of grid harmonics [62–66]. In the case of APD control, it needs to compensate for the power pulsation generated by the grid harmonic voltage v_{gh} in addition to the power pulsation generated by the fundamental component v_{gf}.

The influence of harmonic voltages on the DC voltage ripple is evaluated in this study. From (2.1), the output power p_{AC} is composed of P_{DC} and the power pulsation p_f. However, a single-phase grid voltage has harmonic components v_{gh} in addition to the fundamental

component v_{gf}, as shown in Fig. 2.13. Eq. (2.5) shows the output power p_{ACh} when the grid voltage has the fundamental and 3rd harmonic components.

$$\begin{aligned} p_{ACh} &= i_{AC} \times (v_{ACf} + v_{ACh}) \\ &= \sqrt{2}I_1 \sin\omega_g t \times \sqrt{2}V_1 \sin\omega_g t + \sqrt{2}\mathrm{I}_1 \sin\omega_g t \times \sqrt{2}V_3 \sin 3\omega_g t \\ &= I_1V_1 - I_1V_1 \cos 2\omega_g t + (I_1V_3 \cos 2\omega_g t - I_1V_3 \cos 4\omega_g t) = P_{DC} + p_f + p_h \end{aligned} \quad (2.5)$$

Here, V_3 is the RMS value of the 3rd harmonic voltage and p_h is the output power pulsation caused by the harmonic component. Additionally, the initial phases of the fundamental and harmonic voltage are 0 degrees.

From (2.5), p_{ACh} includes the 2nd and 4th power pulsations caused by the 3rd harmonic voltage in addition to p_f. Fig. 2.14 shows the effect of the 3rd harmonic voltage on the output power pulsation p_{ripple}. The 2nd power pulsation caused by the 3rd harmonic voltage p_{h2} is opposite to that of p_f. Therefore, the 2nd power pulsation $p_{ripple2}$ is reduced. The 2nd and 4th DC voltage ripples are caused by $p_{ripple2}$ and the 4th power pulsation $p_{ripple4}$, as shown in Fig. 2.14.

The 2nd and 4th DC voltage ripples can be expressed by the output power pulsations p_f and p_h and compensating power p_x as in (2.6) and (2.7).

$$\Delta v_{DCrip2} = \frac{(P_f - P_{h2}) - P_{X2}}{\omega_g V_{DC} C_{DC}} = \frac{(P_f - P_{h2}) - cP_f}{\omega_g V_{DC} C_{DC}} \quad (2.6)$$

$$\Delta v_{DCrip4} = \frac{P_{h4}}{2\omega_g V_{DC} C_{DC}} \quad (2.7)$$

Here, the n-th DC voltage ripple Δv_{DCripn} is the peak-to-peak value of the AC component at v_{DC} as shown in Fig. 2.14; P_{Xn} is the amplitude of the n-th compensating power; P_f is the amplitude of the 2nd power pulsation caused by the fundamental component; P_{h2} and P_{h4} are the amplitudes of the 2nd and 4th power pulsation caused by 3rd harmonic component, respectively; V_{DC} is the average DC voltage. Additionally, the initial phase of the fundamental voltage v_{ACf} and harmonic voltage v_{ACh} is 0 degree. The 2nd voltage

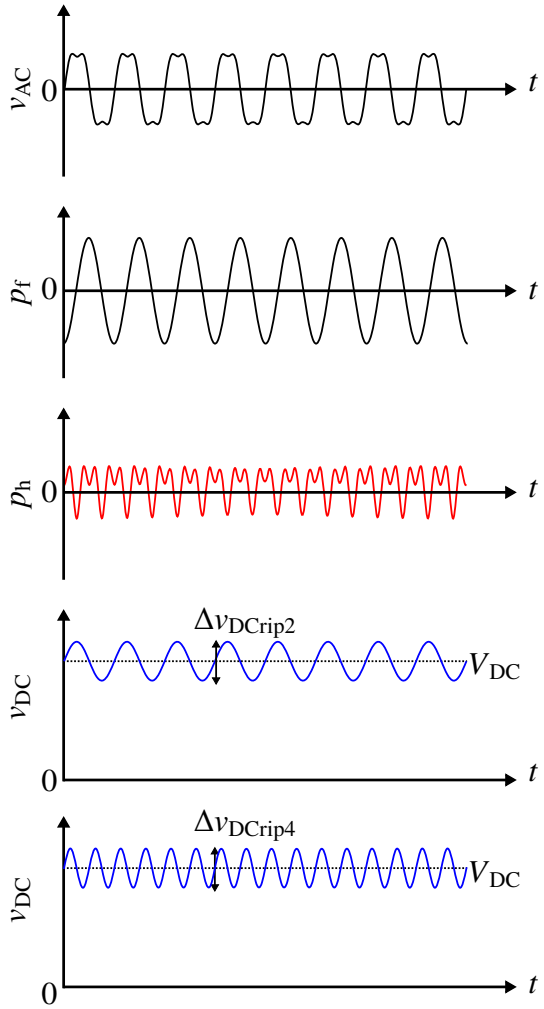


Figure 2.14. Effect of 3rd harmonic voltage on output power pulsation p_{ripple}.

ripple can be controlled by compensating with P_X according to P_f and P_{h2}. Conversely, the 4th voltage ripple is not compensated by P_X; therefore the value is determined by P_{h4}.

Fig. 2.15 shows the voltage ripple ratio generated for the 3rd harmonic voltage at P_{AC} = 1 kW and C_{DC}=50 µF from 2.6 and 2.7. It can be seen that the voltage ripple factor increases as the 3rd harmonic voltage increases. Therefore, APD control that takes harmonics into account is required to achieve a voltage ripple ratio of 5%.

2.3.2 Related study of APD control focus on grid harmonic voltage

The APD control considering grid harmonics has been studied in [67]. Fig. 2.16 shows an inverter with an APD circuit proposed in the literature, and Fig. 2.17 shows its control

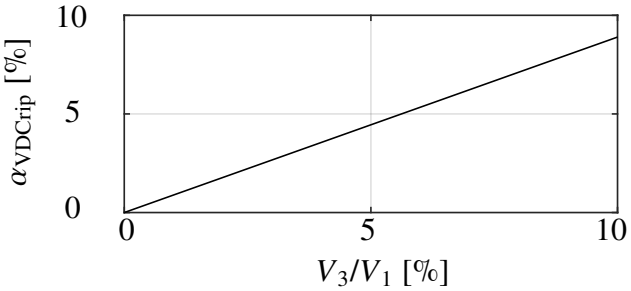


Figure 2.15. Effect of harmonic voltage on voltage rippple

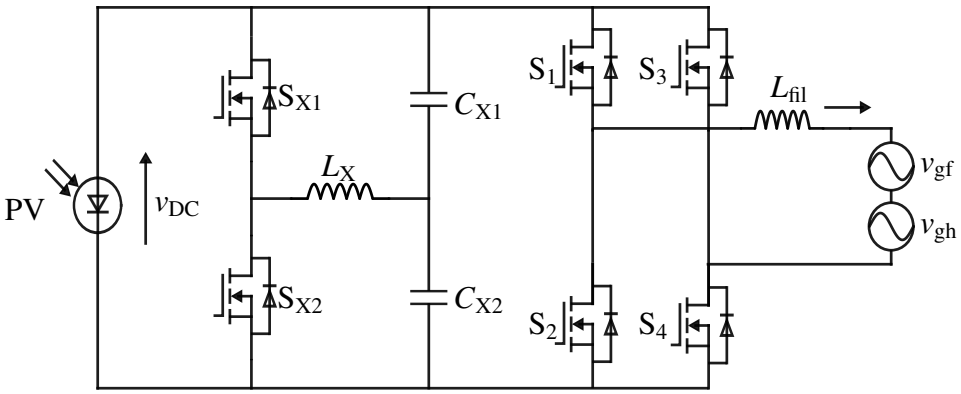


Figure 2.16. APD circuit for harmonic voltage.

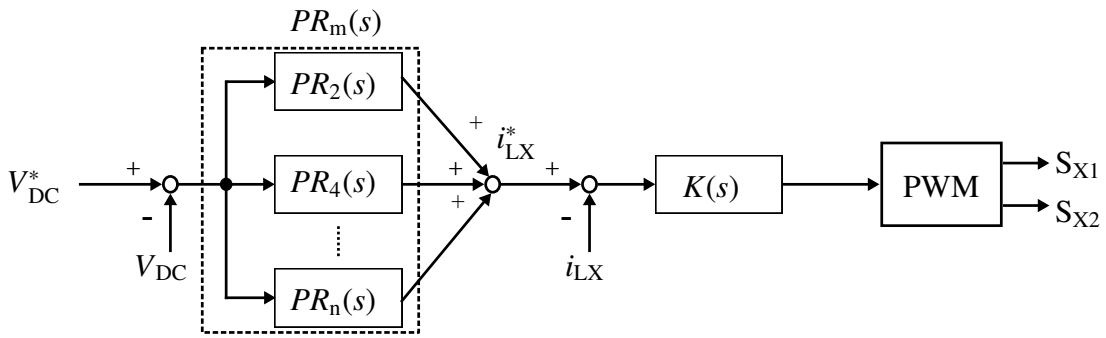


Figure 2.17. APD control for harmonic voltage.

block. The control block in Fig. 2.17 is an APD control based on DC voltage. When system harmonics are present, compensation is required for frequencies above 200 Hz owing to the presence of harmonics in addition to the conventional 100 Hz. The control block uses multiple PR compensators $PR_m(s)$ to provide responsiveness to multiple frequencies. Eq. (2.8) shows the transfer function of $PR_m(s)$.

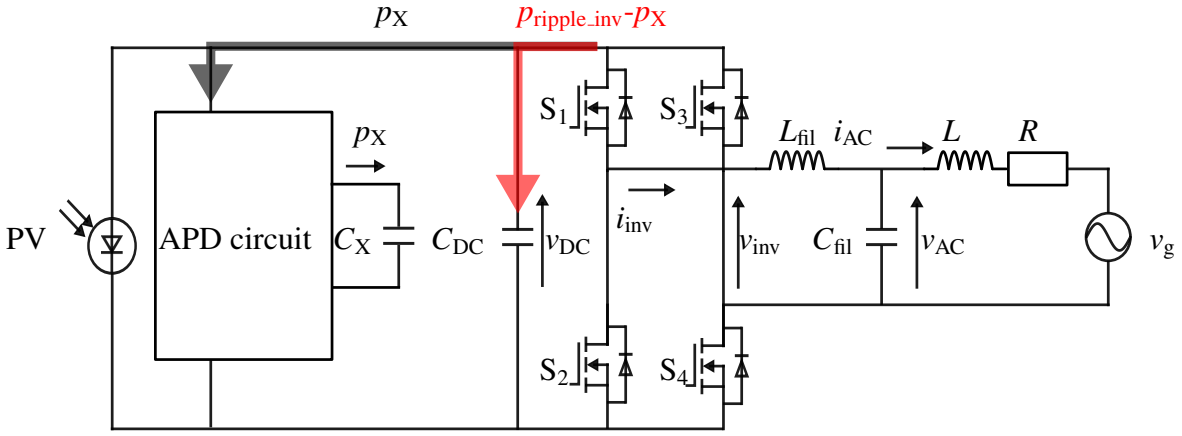


Figure 2.18. APD circuit with grid impedance L, R.

$$PR_m(s) = K_P + \frac{2K_{Ri}\omega_b s}{s^2 + 2\omega_b s + \omega_{hi}^2} \tag{2.8}$$

where ω_{hi} is the target angular frequency and ω_b is the band angular frequency. The target frequency is the even-order frequency of the grid (i=2,4, ...,n).

While the study of APD control based on DC voltage includes grid harmonics, the study of APD control based on power pulsation has not yet been sufficiently considered. A design is required to include power pulsations caused by grid harmonics to realize APD control that achieves a voltage ripple of 5%. Therefore, it is necessary to study APD control based on power pulsation that considers grid harmonics.

2.4 Grid impedance

2.4.1 Effect of grid impedance on APD control

Many studies on grid-connected inverters have reported that grid impedance affects the control stability and performance of inverters [68–75]. The control parameter design is based on an analysis of the effect of grid impedance on the stability of inverter control [68], [69]. The real-time control parameter update method by combining grid impedance estimation and inverter control has been proposed in [74], [75]. During APD control, the power pulsation must be controlled according to the grid impedance of the distribution

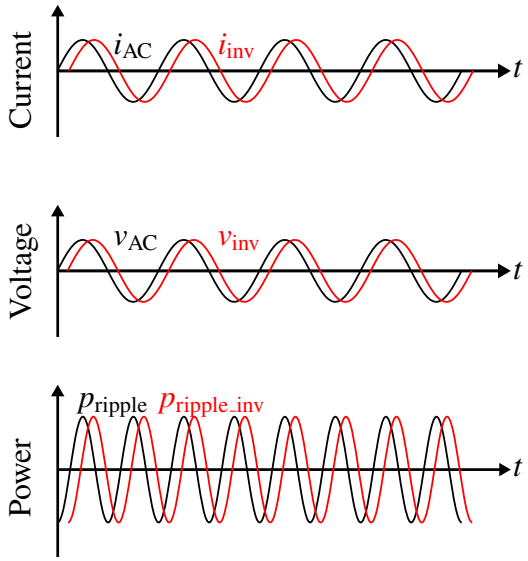


Figure 2.19. Effect of grid impedance on output power pulsation p_{ripple}.

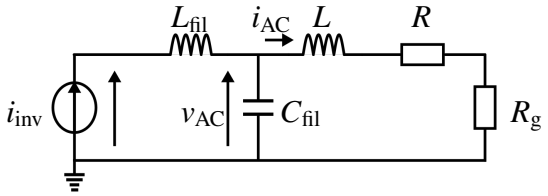


Figure 2.20. Equivalent circuit of grid impedance at 50 Hz.

grid.

The effect of grid impedance on APD control is clarified. As shown in, (2.1) APD control compensates for the pulsation component of the output power. On the other hand, the pulsation component propagated in the DC voltage is generated from the inverter current i_{inv} and the inverter voltage v_{inv}. Fig. 2.19 shows the effect of grid impedance on power pulsation. The phase difference between the current and voltage is caused by the LC filter at the inverter output and the grid impedance L_g. This current and voltage phase difference also causes a phase difference between output power pulsation p_{ripple} and power pulsation propagating in DC voltage p_{ripple_inv}. Eq. (2.9) shows the power pulsation propagated to the DC side p_{ripple_inv}.

$$\begin{aligned} p_{\mathrm{inv}} &= i_{\mathrm{inv}} \times v_{\mathrm{inv}} = \sqrt{2} I_1 \sin(\omega_{\mathrm{g}} t + \Delta\theta_{\mathrm{i}}) \times \sqrt{2} V_1 \sin(\omega_{\mathrm{g}} t + \Delta\theta_{\mathrm{v}}) \\ &= I_1 V_1 \cos(\Delta\theta_{\mathrm{i}} - \Delta\theta_{\mathrm{v}}) - I_1 V_1 \cos(2\omega_{\mathrm{g}} t + \Delta\theta_{\mathrm{i}} + \Delta\theta_{\mathrm{v}}) \\ &= I_1 V_1 \cos(\Delta\theta_{\mathrm{i}} - \Delta\theta_{\mathrm{v}}) - I_1 V_1 \cos(2\omega_{\mathrm{g}} t + \Delta\theta_{\mathrm{p}}) \\ &= P_{\mathrm{DC}} + p_{\mathrm{ripple\_inv}} \end{aligned} \tag{2.9}$$

Here, only the fundamental component is considered for the inverter current i_{inv} and voltage v_{inv}. The $\Delta\theta_{\mathrm{i}}$ represents the phase difference between i_{AC} and i_{inv}, and $\Delta\theta_{\mathrm{v}}$ represents the phase difference between v_{AC} and v_{inv}.

The equivalent circuit at 50 Hz with derivation of the phase relationship is shown in Fig. 2.20. Here, v_{g} is expressed as the resistance R_{g} for the effective power output from the inverter. Each phase difference can be expressed by (2.10) and (2.11) from the LC filter L_{fil}, C_{fil}, and the grid impedance L, R.

$$\Delta\theta_{\mathrm{i}} = \frac{\omega_{\mathrm{g}} C_{\mathrm{fil}} (R + R_{\mathrm{g}})}{1 - \omega_{\mathrm{g}}^2 L C_{\mathrm{fil}}} \tag{2.10}$$

$$\Delta\theta_{\mathrm{v}} = \frac{\omega_{\mathrm{g}} L_{\mathrm{fil}}}{(R + R_{\mathrm{g}})(1 - \omega_{\mathrm{g}}^2 L_{\mathrm{fil}} C_{\mathrm{fil}})} \tag{2.11}$$

From the equations, it can be confirmed that $p_{\mathrm{ripple\_inv}}$ also has a phase difference with p_{ripple} because it contains a phase difference between current and voltage. The compensating power p_{X} of the APD circuit is expressed by (2.12) from the output power p_{AC} and estimated grid impedance L', R'.

$$\begin{aligned} p_{\mathrm{inv}} &= I_1 V_1 \cos(2\omega_{\mathrm{g}} t + \Delta\theta'_{\mathrm{p}}) \\ &= I_1 V_1 \cos(2\omega_{\mathrm{g}} t + \frac{\omega_{\mathrm{g}} C_{\mathrm{fil}} (R' + R_{\mathrm{g}})}{1 - \omega_{\mathrm{g}}^2 L' C_{\mathrm{fil}}} + \frac{\omega_{\mathrm{g}} L_{\mathrm{fil}}}{(R' + R_{\mathrm{g}})(1 - \omega_{\mathrm{g}}^2 L_{\mathrm{fil}} C_{\mathrm{fil}})}) \end{aligned} \tag{2.12}$$

The influence of the grid impedance can be suppressed by APD control that takes the phase difference into account when the grid impedance is known. On the other hand, the grid impedance varies with time. The effect on voltage ripple when there is a difference

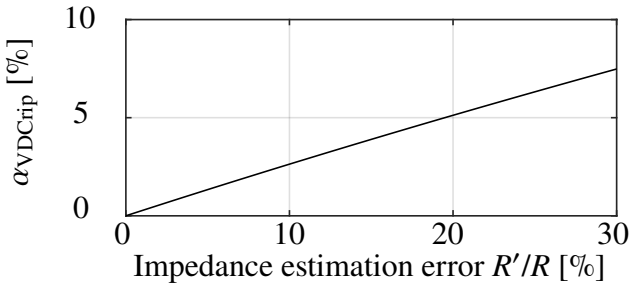


Figure 2.21. Effect of grid impedance estimation error on voltage ripple.

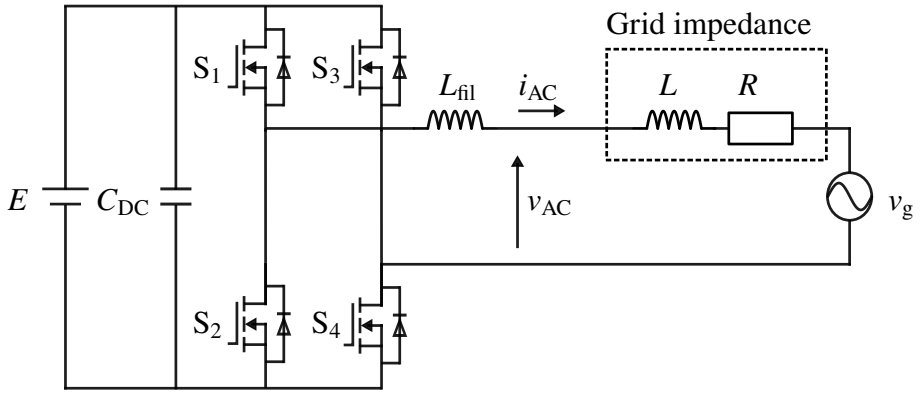


Figure 2.22. Grid impedance estimation for LR component.

between the estimated and actual impedances is expressed by (2.13) from the difference between $p_{\text{ripple\_inv}}$ and p_{X}.

$$\Delta v_{\text{DCrip}} = \frac{I_1 V_1 \{(\cos\theta_{\text{p}} - \cos\theta'_{\text{p}}) + (\sin\theta_{\text{p}} - \sin\theta'_{\text{p}})\}}{\omega_{\text{g}} V_{\text{DC}} C_{\text{DC}}} \tag{2.13}$$

Fig. 2.21 shows the effect of impedance estimation error with respect to R on the voltage ripple ratio at V_1=100 V, I_1=50 A, C_{DC}=50 μF, and V_{DC}=200 V. It can be confirmed that the voltage ripple increases with an increase in the impedance estimation error. Therefore, it is necessary to perform phase compensation of the APD control by accurate impedance estimation.

2.4.2 Related studies on grid impedance estimation

Many studies have been conducted on the estimation of grid impedance [76–90]. Passive and active methods have been proposed for grid impedance estimation. The passive

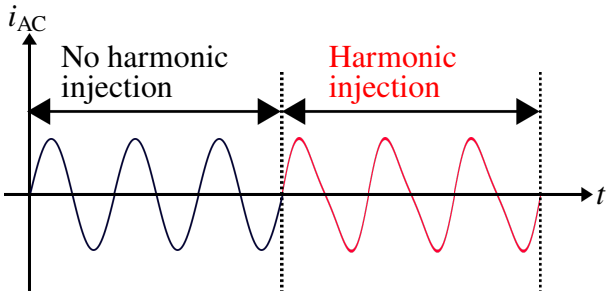


Figure 2.23. Harmonic injection of a single frequency.

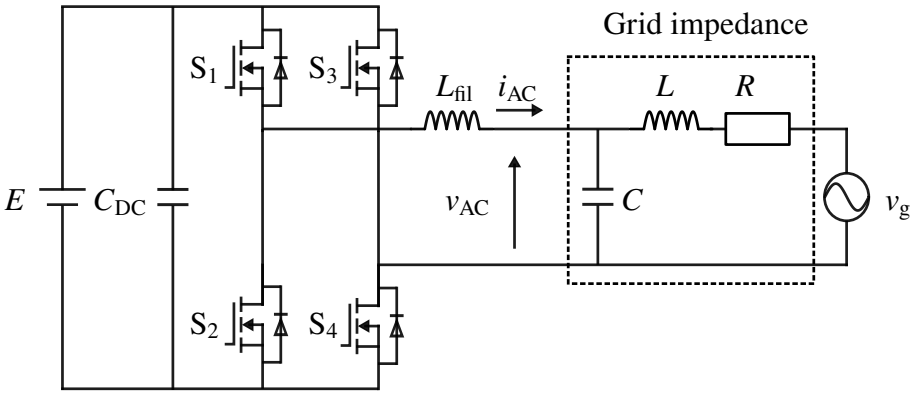


Figure 2.24. Grid impedance estimation for LCR component.

method estimates the grid impedance based on disturbances generated in the grid [76–83]. Although it has low estimation accuracy and cannot estimate the grid impedance at the desired timing, it is useful as an estimation technique that minimizes changes in the grid. The active method estimates the grid impedance based on the changes caused by injecting disturbances into the grid by the inverter control. The active method has the advantage that the estimation can be done at the desired timing, and the estimated frequency range, estimation accuracy, and estimation time can be controlled by design.

Many studies have been conducted on injecting methods that inject harmonic current and voltage into the grid [84–87], as well as methods that change the active and reactive power [88–90]. Fig. 2.22 shows a grid-connected inverter and Fig. 2.23 shows an example of harmonic injection used to estimate the grid impedance. Current control is performed at the grid frequency in the steady state, and harmonic currents are injected during grid impedance estimation to estimate the grid impedance by reading the voltage change.

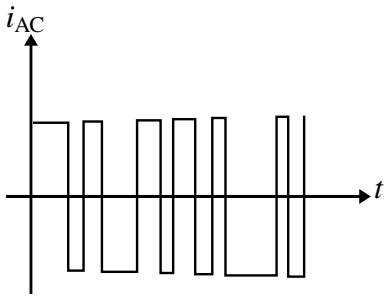


Figure 2.25. Harmonic injection of multiple frequencies.

In the conventional grid impedance estimation, the grid impedance was assumed to comprise inductive and resistive components. However, power factor correction capacitors are used in the grid to improve the power factor, and the grid contains a capacitive component as well. Ref. [91] examines the case in which a power factor correction capacitor and other components resonate with the wiring inductance in a medium-voltage distribution grid, thereby affecting the frequency characteristics between the 2nd and 20th orders. In a low-voltage distribution grid, the capacitive component of the output LC filter of the distributed power supply is increasing. The increase in the capacitive component of the grid causes a resonant element in the grid impedance from the 2nd to 20th order, which affects the inverter control. In addition, references [92], [93] study the impact of grid impedance with the capacitive component on inverter control. Therefore, it is important to include the capacitive component for grid impedance estimation.

Impedance estimation has also been proposed for grid impedance with the resonant elements [94–99]. Ref. [97] reports a highly accurate grid impedance estimation with resonant characteristics in 50.4 s using a technique that injects harmonic currents with multiple frequencies into the grid. Fig. 2.24 shows a grid-connected inverter with grid impedance that has a resonant element at the output, and Fig. 2.25 shows the harmonic currents with multiple frequencies that are used to estimate the grid impedance. It is possible to acquire multiple frequency responses simultaneously by injecting a square wave signal with varying pulse width. As a result, the estimation time is shortened. However, although the grid impedance estimation with resonant elements has realized the acquisition of impedance-frequency characteristics, it has not been able to estimate the inductance,

capacitance, and resistance (LCR parameters). It is important to estimate parameters for grid impedance with resonant elements since there are analyses using parameters such as inductance and capacitance of the grid impedance as in the Refs. [92], [93]. In addition, the grid impedance varies with time because of load conditions and network switching; hence, it is necessary to estimate and update the grid impedance in real time. Parameter estimation is essential to derive the phase difference for APD control. Therefore, the development of parameter estimation techniques for grid impedance with resonant characteristics is required.

2.5 Summary

Chapter 2 reviews related research and clarify issues that require solutions. Many studies on improving the efficiency of the APD method focus on the circuit scheme. On the other hand, there have been very few studies on operation methods, such as controlling the compensating power of the APD circuit based on the operating power and power generation characteristics of the PV array. PV equivalent circuit was used to evaluate the PV power generation efficiency and effect of voltage ripple. Based on the evaluation results, a voltage ripple of 5% is defined as the allowable voltage ripple ratio, and the objective is to realize APD control with compensated power that achieves a voltage ripple of 5%. This dissertation proposes a control scheme to control the compensating power of the APD circuit according to the power generation characteristics of the PV array to achieve higher efficiency for the PV system.

The effect of partial shade on the power generation efficiency of a PV array was shown. As a partial shade suppression method, GCC using a power conversion circuit is presented, and it is shown that by controlling the operating point of each PV module, maximum power can be produced even under the influence of partial shade. The importance of considering an integrated system of the partial shade compensation and APD method was demonstrated by describing GCC.

The impact of grid harmonic voltage on APD control was clarified, and the study of including power pulsation caused by grid harmonic voltage in voltage control was shown

to be necessary. Numerical analysis shows that the 3rd harmonic voltage cause 2nd and 4th power pulsations, and that these power pulsations cause DC voltage ripple. The effect of the 3rd harmonic voltage at 1 kW on voltage ripple control is shown, and it is shown that power pulsation caused by harmonic voltage must be considered to achieve a voltage ripple ratio of 5%.

The influence of grid impedance on APD control was clarified, and the technique for obtaining grid impedance in real time was shown to be necessary. The equivalent circuit and numerical analysis at 50 Hz show that the grid impedance parameter is necessary for voltage ripple control. In addition, the effect of grid impedance estimation error on voltage ripple control at 5 kW is shown, indicating that accurate grid impedance estimation is necessary to achieve a voltage ripple ratio of 5%. Furthermore, literature on conventional grid impedance was reviewed, and it was confirmed that most of the literature focus on the resistive and inductive components. In addition, it was confirmed that some studies included the capacitive component in the grid impedance. Because parameter estimation is essential to derive the phase difference for APD control, it is necessary to develop a parameter estimation technique for grid impedance with resonant characteristics.

Chapter 3

Voltage Ripple Control Focusing on PV Power Generation Efficiency

Chapter 3 proposes an APD control considering the power generation characteristics of a PV array. The APD control achieves compensated power control according to the power generated by the PV. Real-time simulation and experimental results for an inverter with a rating of 1 kW will clarify the difference and usefulness of the pulsation compensation of the APD circuit according to the design method of the DC capacitance.

3.1 Main circuit configuration

Fig. 3.1 shows the main circuit configuration and Table 3.1 lists the circuit specifications. The APD circuit is a buck-boost converter consisting of a decoupling capacitor C_X,

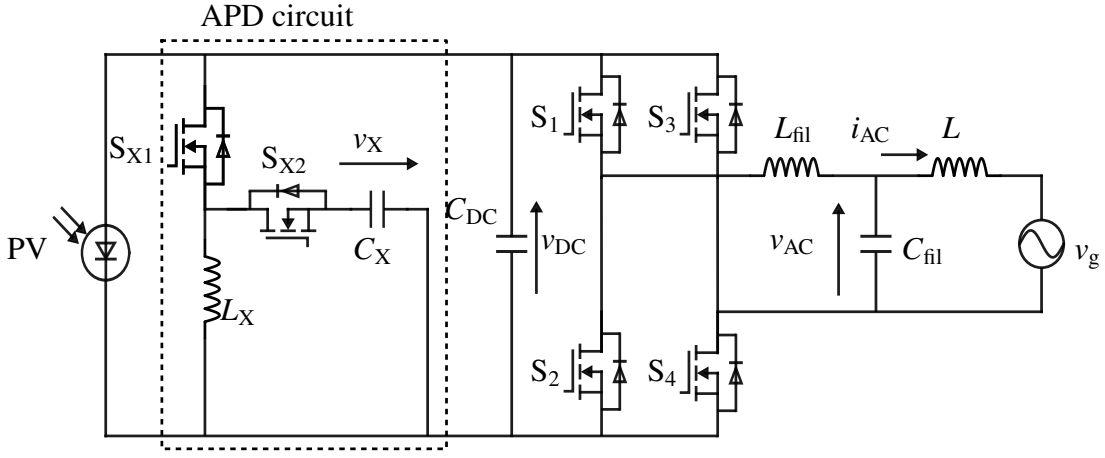


Figure 3.1. Main circuit configuration of APD circuit.

Table 3.1. Circuit specification and parameters.

Parameter	Value
Grid voltage v_g	100 V
Grid frequency f_{grid}	50 Hz
Input voltage V_{DC}	180 - 200 V
Decoupling average voltage V_{Xave}	300 V
Input capacitance C_{DC}	50, 300 µF
LC filter inductance L_{fil}	2250 µH
LC filter capacitance C_{fil}	3.3 µF
Grid inductance L	100 µH
Decoupling inductance L_X	1600 µH
Decoupling capacitance C_X	50 µF
APD switching frequency f_{sAPD}	20 kHz
Inverter switching frequency f_{sinv}	20 kHz

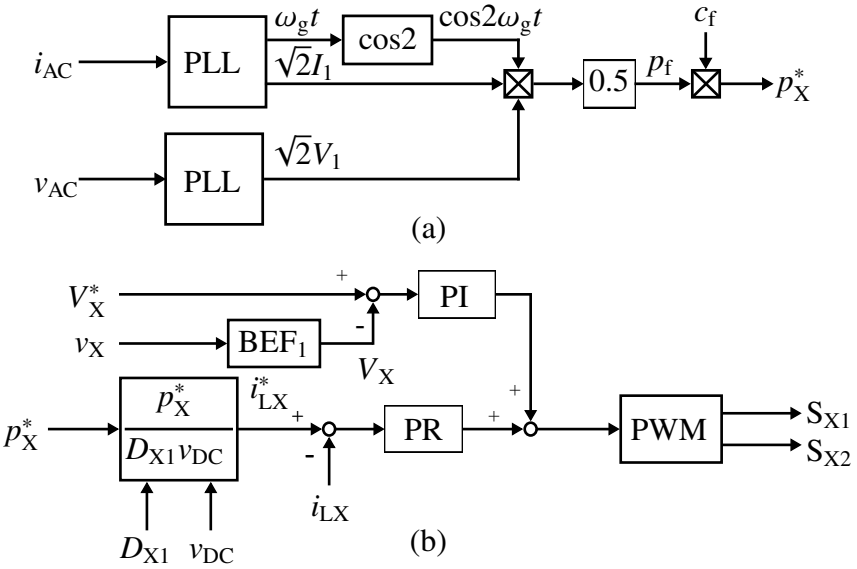


Figure 3.2. Block diagram of the APD control. (a) Compensating power calculation block. (b) Control block of inductor current i_{LX} and average decoupling capacitor voltage V_X.

decoupling inductor L_X, and switches S_{X1}, S_{X2}.

3.2 Voltage ripple control using compensation ratio c_f

3.2.1 APD control block

Fig. 3.2 shows the proposed APD control block and Table 3.2 lists the control parameters.

In the proposed APD control, the compensating power p_X is controlled from the inductor

Table 3.2. Control parameters of conventional APD control.

Parameter	Value
Resonant gain K_R	100
Proportional gain K_P	20
Resonant angular frequency ω_0	2*π*100 rad/s
Band angular frequency ω_b	2*π*10 rad/s
Eliminated angular frequency 1 ω_{e1}	2*π*100 rad/s
Band angular frequency 1 ω_{b1}	2*π*10 rad/s

current command value i^*_{LX} and the average value of the decoupling capacitor voltage V_X is controlled from the average value command V^*_X. The conventional APD control always uses the output power pulsation p_{ripple} to calculate i^*_{LX} for maximum compensation, the proposed APD control introduces a compensation ratio c_f that varies between 1 and 0, so that the control is performed at p_X, where the voltage ripple ratio of v_{DC} α_{DCrip} operates at the allowable ripple ratio according to the operating power. When c_f=0, i.e., p_X=0, the compensating power control and the average value control of the decoupling capacitor voltage are stopped.

Fig. 3.2(a) shows the compensating power calculation block. The amplitudes V_1, I_1 and phase of the fundamental component $\omega_g t$ are obtained from the output voltage v_{AC} and output current i_{AC} using a phase-locked loop(PLL) [100]. The compensating power command p^*_X is calculated from V_1, I_1, $\omega_g t$, and c_f.

Fig. 3.2(b) shows the control block of the inductor current i_{LX} and average decoupling capacitor voltage V_X. The inductor current command i^*_{LX} is calculated from p^*_X, DC voltage v_{DC}, and duty ratio D_{X1} of switch S_{X1}. The inductor current i_{LX} follows i^*_{LX} in a feedback loop using a proportional-resonant (PR) compensator PR. The compensating power p_X is charged and discharged to C_X by controlling i_{LX}. Eq. (3.1) shows the transfer function of PR [101–103].

$$PR(s) = K_P + K_R \frac{2\omega_b s}{s^2 + 2\omega_b s + \omega_0^2} \tag{3.1}$$

In the average value control, the average value of the decoupling capacitor voltage V_X

Table 3.3. Inductor specifications.

Parameter	Value
Core volume	48.4 cc
AL value	146 nH
Magnetic circuit length l_e	0.146 m
Number of turns N	61
Number of cores m	3

follows the command V_X^* in a feedback loop using a proportional-integral compensator. V_X is detected by removing the 100 Hz component from v_X using the band elimination filter BEF_1. Eq. (3.2) shows the transfer function of BEF_n.

$$BEF_n(s) = \frac{s^2 + \omega_{en}^2}{s^2 + 2\omega_{bn}s + \omega_{en}^2} \tag{3.2}$$

3.2.2 Design of decoupling indctor L_X

The decoupling inductance L_{Lx} is designed based on the inductor current ripple. Because the amplitude of the inductor current ripple is largest for the 100 Hz component, the design focuses on the 100 Hz component. Eq. (3.3) shows the relationship between the inductor current ripple and inductance L_X. The inductance is calculated as the inductor current ripple $\Delta I_{100peak}$ caused by the switching frequency in relation to the current peak $I_{LX,\,SW}$ is set to be 1600 µH as the value that is within 50 % or less.

$$I_{100peak} \times 0.5 \geq \Delta i_{LX,\,SW} = \frac{V_{DC} \times D_{X1} \times T_{SW}}{L_X} \tag{3.3}$$

where T_{SW} is the switching time of one cycle. Table 3.3 lists the inductor specifications. Eq. (3.4) shows the relationship between the number of inductor turns N and the magnetic flux H.

$$4500 \geq H = \frac{N \times I_{LXpeak}}{l_e} \tag{3.4}$$

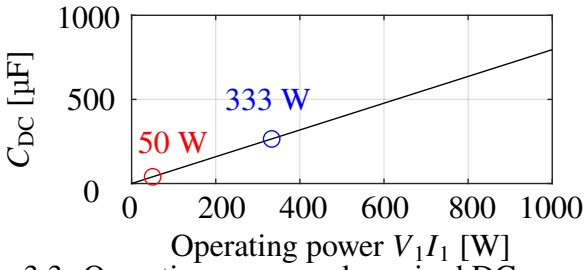


Figure 3.3. Operating power and required DC capacitance C_{DC}

Where I_{LXpeak} is the peak value of the inductor current i_{LX} and l_e is the average magnetic path length of the toroidal core. Eq. (3.5) is the relationship between the inductance L_X, value of AL, and number of turns N.

$$L_X = 1600 \times 10^{-6} = \mathrm{AL} \times m \times N^2 \tag{3.5}$$

Since I_{LXpeak} is 10.21 A when operating at 1 kW, the number of turns N satisfying equations (3.4) and (3.5) is 61 and the number of cores m is 3.

3.2.3 Design of the DC capacitance C_{DC}

The capacitance of the DC capacitor C_{DC} is derived from the design that focuses on the 100 Hz voltage ripple $\Delta v_{rip,\,100}$ when the APD control is stopped to improve the system efficiency of the inverter. Eq. (3.6) shows the relationship between C_{DC} and $\Delta v_{rip,\,100}$.

$$C_{DC} = \frac{V_1 I_1}{\omega V_{DC} \Delta v_{rip,\,100}} \tag{3.6}$$

where ω is the grid angular frequency. Fig. 3.3 shows the capacitance required to achieve α_{VDCrip}=5% when the APD circuit is stopped, relative to the amount of operating power $V_{AC} I_{AC}$. C_{DC}=50 μF is required for 50 W and C_{DC}=300 μF for 333 W. The system efficiency of the proposed APD control system is verified when 50 and 300 μF derived for C_{DC} are used.

3.2.4 Design of decoupling capacitor C_{X}

The capacitance of the decoupling capacitor C_{X} is designed based on the compensating power p_{X} and the decoupling capacitor voltage v_{X} when operating at the rated 1 kW. Since the APD circuit is a buck-boost converter, the relationship between the inverter input voltage v_{DC} and the average voltage V_{X} of the decoupling capacitor voltage can be expressed by (3.7).

$$V_{\mathrm{Xave}} = \frac{D_{\mathrm{X1}}}{1 - D_{\mathrm{X1}}} V_{\mathrm{DC}} \tag{3.7}$$

The ratio of p_{X} to the power pulsation p_{ripple} in (3.8) is defined as the compensated power ratio CP_{ratio}.

$$CP_{\mathrm{ratio}} = \frac{P_{\mathrm{X}}}{P_{\mathrm{ripple}}} \times 100 \tag{3.8}$$

Eq. (3.9) shows the relationship between the decoupling capacitor voltage v_{X}, compensation power p_{X}, and C_{X}.

$$C_{\mathrm{X}} = \frac{CP_{\mathrm{ratio}} V_1 I_1}{\omega V_{\mathrm{Xave}} \Delta v_{\mathrm{Xrip}}} \tag{3.9}$$

where Δv_{Xrip} is the ripple component of the decoupling capacitor voltage. From (3.9), when V_{X}=300 V, CP_{ratio}=100%, V_1=100 V, I_1=10 A, a capacitor capacitance of C_{X}=50 µF is required to achieve Δv_{Xrip}=200 V. The C_{X}=50 µF is applied under all operating conditions as in the conventional APD control, and control is performed with V_{X}=300 V constant.

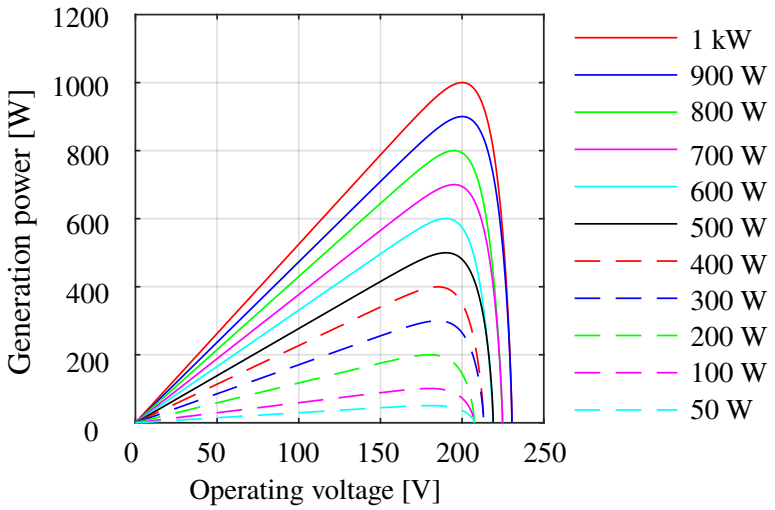


Figure 3.4. PV characteristics of 100 W – 1 kW for real-time simulation.

3.3 Relationship between DC voltage ripple and compensation ratio c_f

3.3.1 Verification system of real-time simulator

It is difficult to verify the control strategies because the power generation characteristics depend on the actual experimental environment. Therefore, the influence of the harmonic voltage on the conventional APD control is verified through real-time simulation. Fig. 3.5 shows the verification system configuration. The main circuit operation is calculated by the hardware-in-the-loop (HIL) simulator (HIL402) from Typhoon HIL. The inverter and APD controls were executed by a microcontroller (TMS320F28379D) from Texas Instruments. Fig. 3.4 shows the P-V characteristics for real-time simulation. The power generation characteristics of each PV array are calculated in HIL402. For each PV array generating 50 W–1 kW, the power generation efficiency of the PV array for each capacitance is calculated.

3.3.2 Verification result of real-time simulations

The voltage ripple response of the APD circuit to the compensating power p_X is verified from real-time simulations. Fig. 3.6 shows the operating waveforms of the compensating

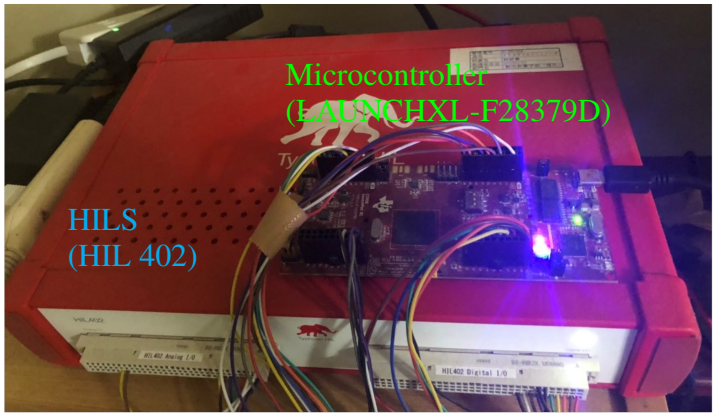


Figure 3.5. Verification system configuration.

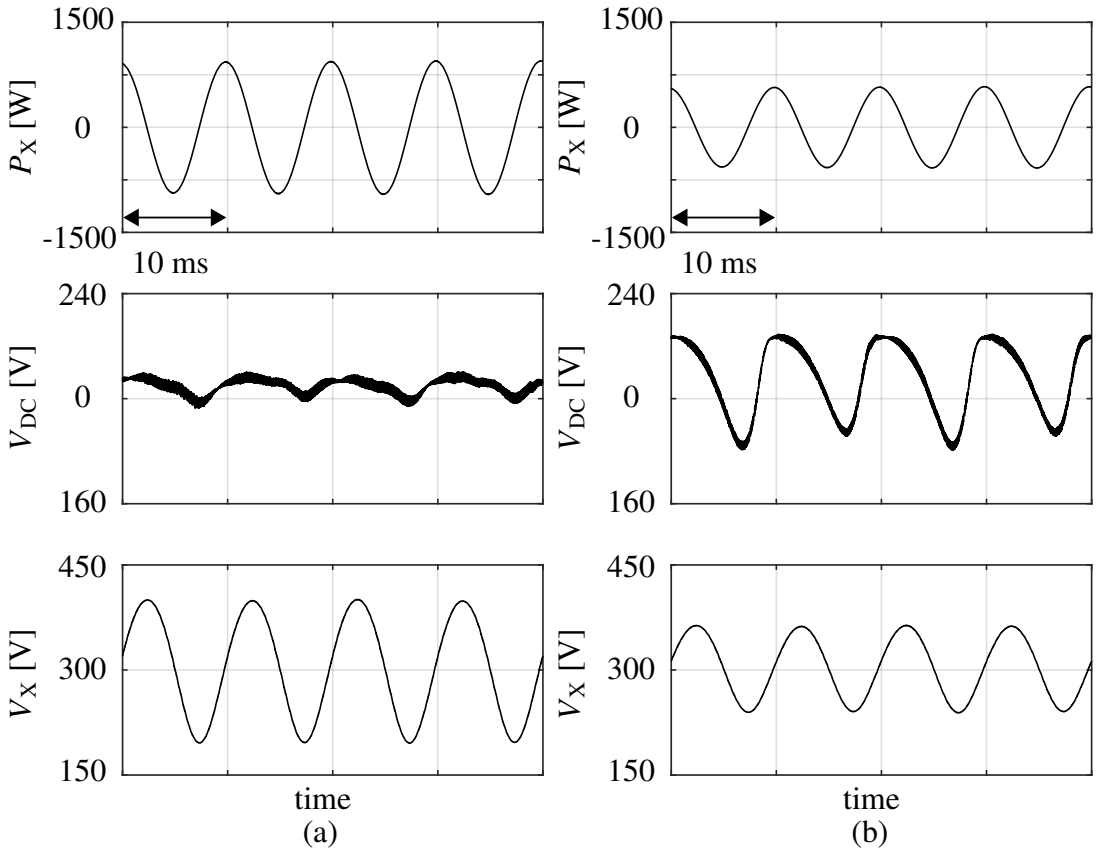


Figure 3.6. Real-time simulation waveform at C_{DC}=50 µF and 1 kW. (a) c_f=1.0. (b)c_f=0.7.

power p_X, DC voltage v_{DC}, and decoupling capacitor voltage v_X when the DC capacitance C_{DC}=50 µF, 1 kW operation. From the waveform of p_X, it can be confirmed that p_X changes according to CP_{ratio}. v_{DC} waveform shows that when CP_{ratio}=100 %, the voltage ripple ratio α_{VDCrip} is suppressed to 5%. On the other hand, when CP_{ratio}=70%, the α_{VDCrip} is more than 5 %, and the change of voltage ripple according to CP_{ratio} can be confirmed.

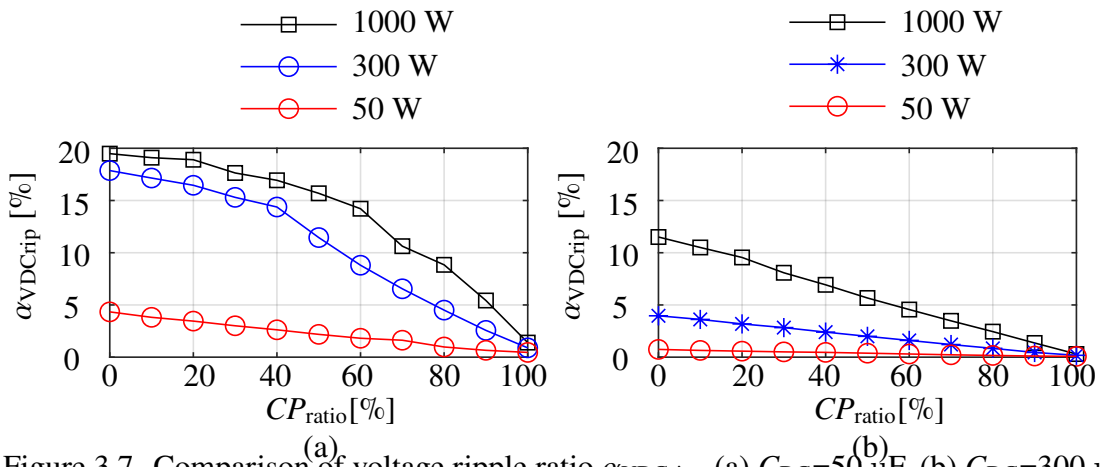


Figure 3.7. Comparison of voltage ripple ratio α_{VDCrip}. (a) C_{DC}=50 µF. (b) C_{DC}=300 µF

The waveform of v_X shows that the average value V_X is controlled at 300 V regardless of CP_{ratio}.

Fig. 3.7 shows the relationship between CP_{ratio} and α_{VDCrip}. Fig. 3.7(a) shows the variation of α_{VDCrip} with CP_{ratio} for each operating power when C_{DC}=50 µF. At 1 kW and 300 W operation, α_{VDCrip} exceeds 5 % as CP_{ratio} decreases. Therefore, to maximize the power generation efficiency, it is necessary to operate with a CP_{ratio} of 100%. On the other hand, at 50 W, α_{VDCrip} remains below 5 % for all CP_{ratio} including the shutdown of the APD circuit. Therefore, even without compensation of the APD circuit, the power generation efficiency is drawn out and the system efficiency improvement is achieved by suppressing the power loss of the APD circuit. Fig. 3.7(b) shows the change of α_{VDCrip} for each CP_{ratio} for each operating power when C_{DC}=300 µF. Because the α_{VDCrip} remains below 5% for all CP_{ratio} below 300 W, the system efficiency is improved over a wide operating power range owing to the shutdown of the APD circuit. At 1 kW operation, the α_{VDCrip} remains below 5% for CP_{ratio} between 70–100%, which means that maximum power generation efficiency can be achieved even at a CP_{ratio} of 70%. From the above results, the CP_{ratio} that can maximize the power generation efficiency varies depending on the operating power and DC capacitance.

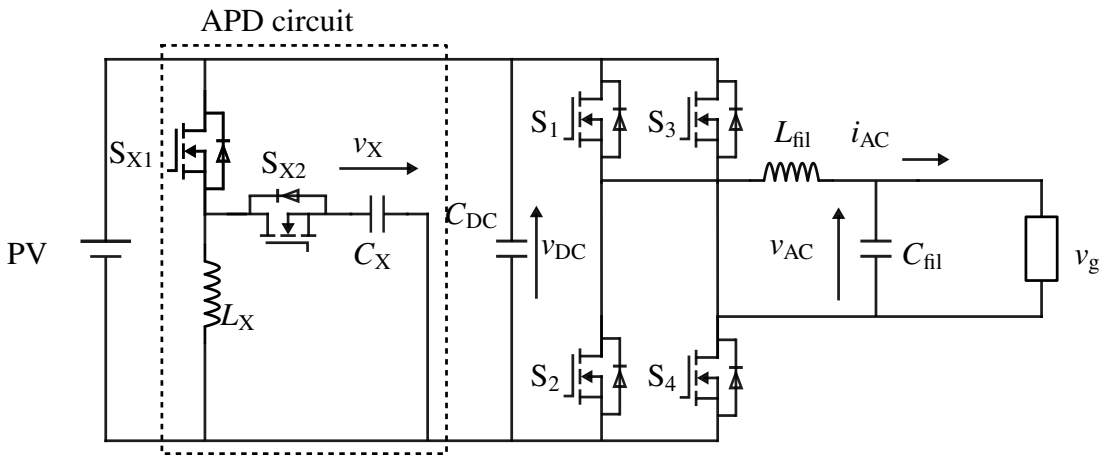


Figure 3.8. Experiment configuration of APD circuit.

Table 3.4. Circuit parameters and model number.

Parameter	Model number
Electric load R_g	PCZ1000A(KIKUSUI)
Film capacitor C_{DC}, C_X	C4AQLBW5500A3JK (KEMET)
Film capacitor C_f	FTACD801V335JTLJZ0 (NIPPON CHEMI-CON)
Inverter switch S_1 - S_4 (GaN-FET)	TPH3212PS(transphorm)
APD switch S_{X1}, S_{X2} (SiC-MOSFET)	SCT2160KEC(ROHM)

3.4 Evaluation of system efficiency of PV system

3.4.1 Experimental Circuit Configuration

Fig. 3.8 shows the experimental circuit configuration of the PV system. Table 3.4 lists the components used in the actual circuit. In the experimental verification, a regulated DC power supply was used as input and an electronic load as output to measure the power conversion efficiency. Because the total voltage of v_{DC} and v_X is applied to the switching device S_{X1}, S_{X2} in the APD circuit, a maximum of 600 V is applied to the device when operating at 1 kW and CP_{ratio}=100%. Therefore, SiC-MOSFETs with a withstand voltage of 1200 V were used. The inverter circuit consists of two half-bridge modules (Transphorm: TDHBG2500P100) that use GaN-FETs.

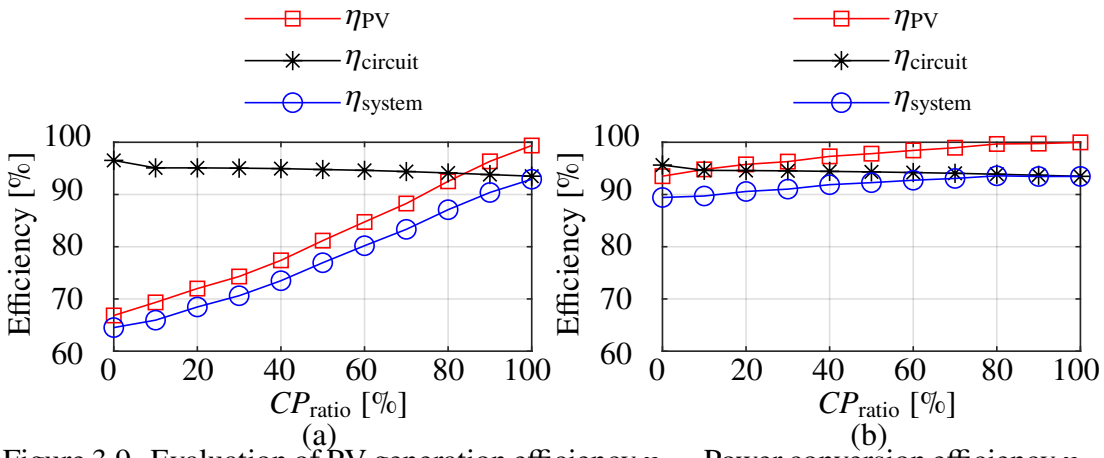


Figure 3.9. Evaluation of PV generation efficiency η_{PV}, Power conversion efficiency η_{circuit} and system efficiency η_{system}. (a) Efficiency of 1 kW at C_{DC}=50 µF. (b) Efficiency of 1 kW at C_{DC}=300 µF.

3.4.2 Evaluation of system efficiency of the APD control

The system efficiency η_{system} is evaluated using the PV power generation efficiency η_{PV} obtained from real-time simulation and the power conversion efficiency η_{circuit} obtained from actual equipment verification. The power conversion efficiency η_{circuit} is defined by equation (3.10), and the system efficiency η_{system} is defined by equation (3.11) as the product of the power conversion efficiency and power generation efficiency. Here, p_{AC} is the output power.

$$\eta_{\mathrm{circuit}} = \frac{p_{\mathrm{AC}}}{P_{\mathrm{PV}}} \times 100 \tag{3.10}$$

$$\eta_{\mathrm{system}} = \frac{\eta_{\mathrm{circuit}}\eta_{\mathrm{PV}}}{100} \tag{3.11}$$

Fig. 3.9(a) shows the efficiency at C_{DC}=50 µF, 1 kW operation, and Fig. 3.9(b) shows the efficiency at C_{DC}=300 µF, 1 kW operation. At C_{DC}=50 µF, 1 kW, there is a significant decrease in power generation efficiency because α_{VDCrip} increases significantly with respect to the decrease in CP_{ratio}. Therefore, it can be confirmed that owing to the large influence of the generation efficiency on system efficiency, the improvement in power conversion efficiency with the decrease in compensation power is not effective, and the

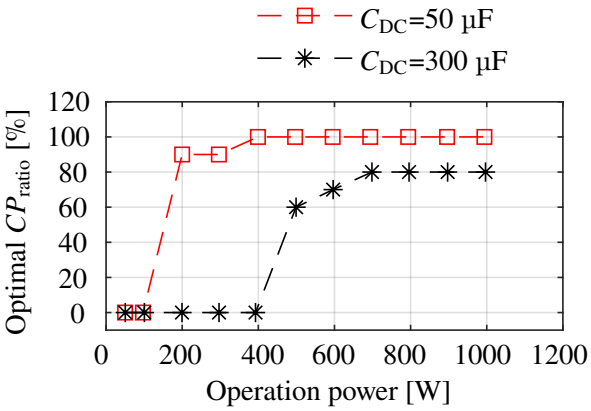


Figure 3.10. Relationship between Compensating power ratio and Operation power.

optimal point is CP_{ratio}=100%. On the other hand, when C_{DC}=300 µF, 1 kW, the decrease in power generation efficiency with respect to the decrease in CP_{ratio} is suppressed as the DC capacitance. As a result, it can be confirmed that CP_{ratio}=80% is optimal owing to the improvement in power conversion efficiency.

Fig. 3.10 shows the variation of the optimal compensation ratio with operating power for each DC capacitance. When C_{DC}=50 µF, it is optimal to stop the APD control at light loads of 50–100 W. On the other hand, 400 W–1 kW requires a CP_{ratio} of 100 % for the APD circuit. At C_{DC}=300 µF, the trend changes and the optimal compensation ratio is suppressed to 80% at 700 W and above. The optimal compensation ratio at 1 kW rating is considered. Because the maximum current capacity of the APD circuit can be reduced to 80% of the 1 kW maximum compensation, switching devices with lower current ratings can be applied compared to the conventional APD control. From the above results, it can be confirmed that the optimum compensation ratio changes according to the DC capacitance and operating power and the maximum current capacity in the APD circuit is suppressed to 80% at C_{DC}=300 kW.

Fig. 3.11 shows the comparison of system efficiency between the proposed APD control and the conventional APD control for each DC capacitance. Fig. 3.11(a) shows that when C_{DC}=50 µF, the efficiency improves by 6.4–16% at 50–100 W owing to the elimination of losses in the inductor and switching devices in the APD circuit as the switching operation of the APD circuit stops. When C_{DC}=300 µF in Fig. 3.11(b), the system efficiency

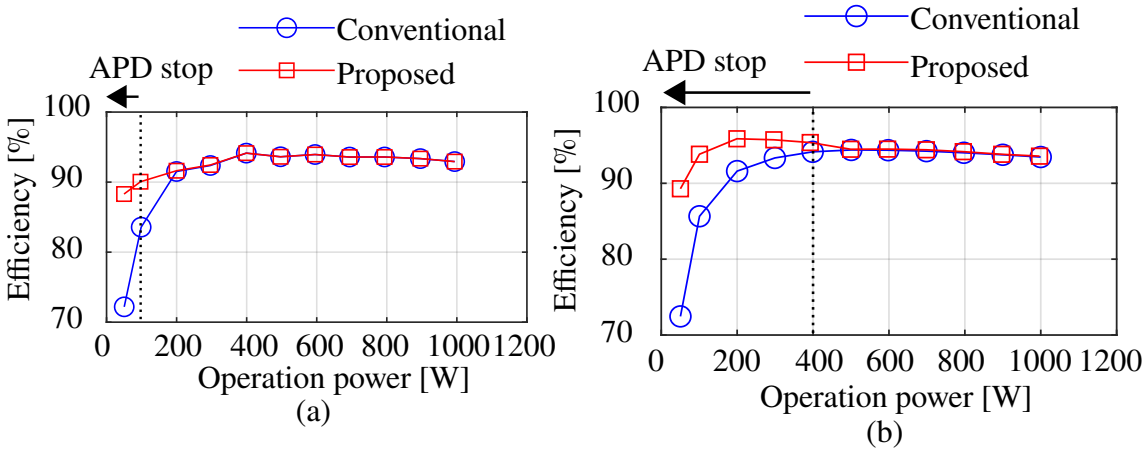


Figure 3.11. Comparison of system efficiency η_{system} between proposed and conventional APD control. (a) C_{DC}=50 µF. (b) C_{DC}=300 µF.

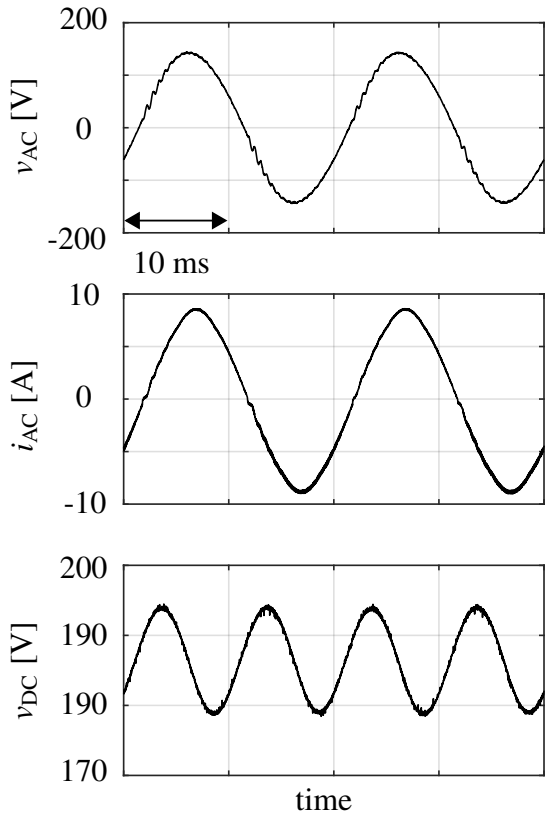


Figure 3.12. Output current i_{AC}.

improves by 1.2–16.8% as the APD circuit is stopped in the range of 400 W and below, as in the case of C_{DC}=50 µF. In addition, Refs. [36] and [38] compare the PV system losses with and without APD circuits, and show that the loss of the APD circuit tends to account for a larger proportion of the total PV system loss at light loads. Therefore, the increase in

efficiency from 400 W to 200 W is owing to the large ratio of the loss of the APD circuit to the total loss of the PV system at light loads. Based on the above results, it can be said that the proposed APD control is an effective method for improving system efficiency at light loads, and it is significant in seasons and regions with long operating hours at light loads.

The effect of the APD control stop on the inverter operation is verified based on the operation results at C_{DC}=300 µF and 300 W. The series resistors of 12 Ω is inserted to the DC power supply E and R reproduce the voltage ripple equivalent to the real-time simulation in v_{DC}. Fig. 3.12 shows the DC voltage v_{DC}, the inverter output voltage v_{AC}, and the inverter output current i_{AC}. A voltage ripple of 3.78% is generated from the DC voltage, but the inverter voltage and current show that the inverter operation is unaffected by the voltage ripple. These results confirm that the proposed APD control improves the system efficiency of the PV system.

3.5 Summary

In chapter 3, the compensating power control for APD control focusing on PV power generation characteristics is proposed. In a 1 kW rated inverter, the difference and usefulness of the pulsation compensation of the proposed APD control were verified for two capacitance design methods: When C_{DC}=50 µF, the compensation power of 100 % by the APD control is required at rated power, but this is much lower than that of 300 µF. The APD control is effective in downsizing the inverter because it uses a small capacitor. On the other hand, when C_{DC}=300 µF, although the capacitance increases, the maximum current capacity is suppressed to 80% of 1 kW operation, enabling the use of switching devices with lower current capacity than in the conventional APD control. In addition, the system efficiency is improved by 1.2–16.8% at an operating power of 400 W or less. This is significant in seasons and regions with low solar radiation and long hours of light-load operations. These results show the difference in the amount of compensating power and the usefulness of the proposed APD control depending on the design method of the DC capacitance.

Chapter 4

PV system with Active Power Decoupling and Generation Control Features

This chapter analyzes two circuit configurations of the PV system equipped active power decoupling and generation control features using the state-space averaging method, and clarifies the difference between the characteristics of the two circuit configurations.

4.1 Main circuit and operation principle of GCC

4.1.1 Main circuit configuration

Fig. 4.1 shows the main circuit configuration of the single-phase inverter with circuit integrating GCC and APD circuit (hereinafter referred to as ”Integrated circuits”). Fig. 4.2 shows the main configuration of the PV system with a combination of the conventional GCC and APD circuits (hereinafter referred to as ”Individual circuit”). The circuit specifications and parameters of both configurations are listed in Table 4.1.

In both systems, the DC power generated by the PV array transmits AC power to the grid via an inverter circuit, and the GCC section controls the operating points of the PV modules individually using switching operations to suppress the effects of partial shading. The active power decoupling circuit section charges and discharges power pulsation to the

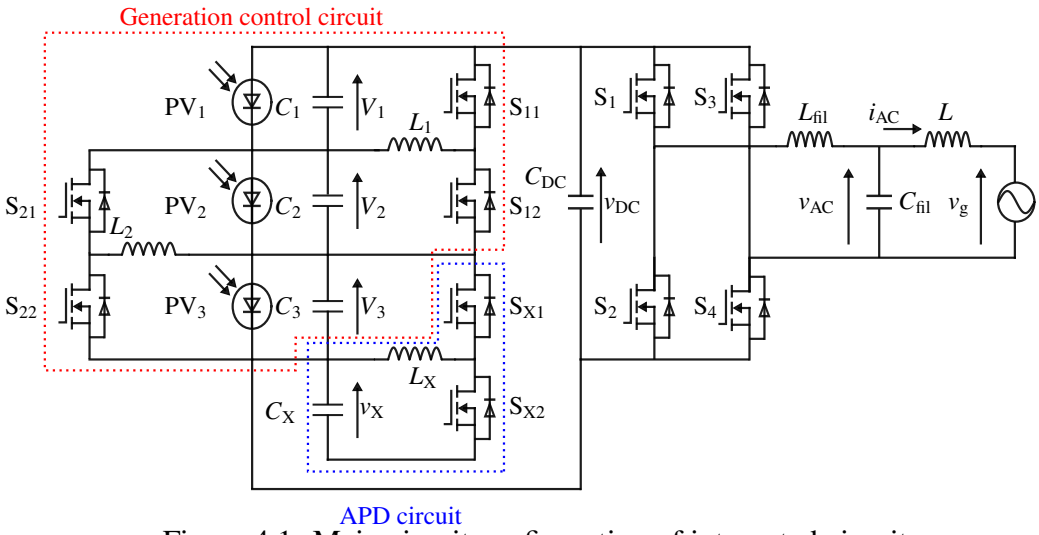


Figure 4.1. Main circuit configuration of integrated circuit.

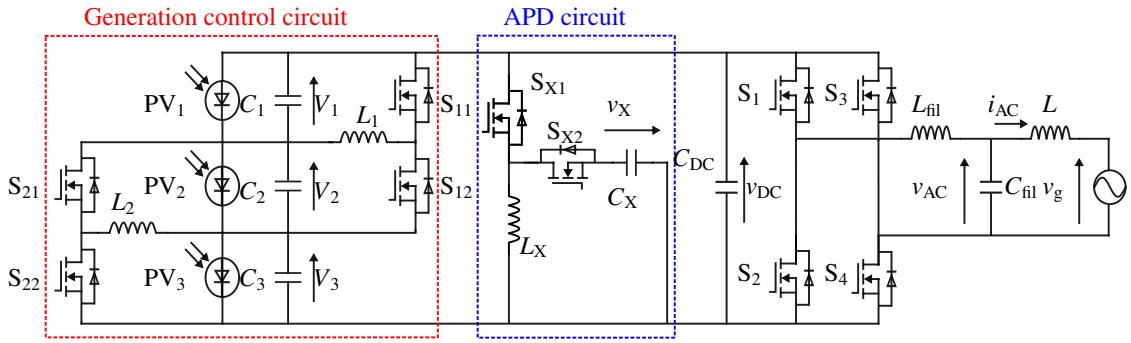


Figure 4.2. Main circuit configuration of individual circuit.

decoupling capacitor C_X through the switching operation of power devices S_{X1} and S_{X2}. The following three characteristics of the integrated circuit and individual circuit can be mentioned.

- In the individual circuit, the sum of the DC voltage V_{DC} and the decoupling capacitor voltage V_X is applied to S_{X1} and S_{X2} used in the power decoupling circuit section; hence, it is necessary to use devices with appropriate withstand voltage values. Because high withstand voltage devices have high conduction resistance, and high voltage operation increases switching losses, V_X must be operated at a relatively low voltage. In the individual circuit, the power decoupling circuit is connected to the DC bus; therefore V_X must be operated at a high boost/buck ratio to operate at a low voltage. Generally, the power conversion efficiency of a buck-boost converter tends

Table 4.1. Circuit specification and parameters of integrated and individual circuits.

Parameter	Value
Grid voltage v_g	100 V
Grid frequency f_{grid}	50 Hz
DC voltage V_{DC}	210 V
Decoupling average voltage of integrated circuit V_{Xave}	240 V
Decoupling average voltage of individual circuit V_{Xave}	315 V
DC capacitance C_{DC}	50 µF
LC filter inductance L_{fil}	2250 µH
LC filter capacitance C_{fil}	3.3 µF
Grid inductance L	100 µH
Decoupling inductance for integrated circuit L_X	800 µH
Decoupling inductance for individual circuit L_X	1600 µH
Decoupling capacitance for integrated circuit C_X	100 µF
Decoupling capacitance for individual circuit C_X	50 µF
GCC inductance L_1, L_2	100 µH
GCC capacitance C_1–C_3	30 µF
APD switching frequency f_{sAPD}	20 kHz
GCC switching frequency f_{sGCC}	40 kHz
Inverter switching frequency f_{sinv}	20 kHz

to decrease as the boost/buck ratio increases, and so operating V_X at a low voltage leads to increased power loss in the power decoupling circuit. In contrast, in the integrated circuit, because the power decoupling circuit is connected to the lowest PV module (PV3), V_X operates at a relatively low boost/buck ratio corresponding to the PV module voltage V_X, and the withstand voltage required for power devices is also low. Therefore, switching loss suppression of S_{X1} and S_{X2} can be expected in the integrated circuit.

- In the integrated circuit, the decoupling inductor L_X is expected to be compact and low-loss. In the individual circuit, since V_X and V_{DC} are applied to L_X, the required inductance becomes large to operate at the same switching frequency and to keep the inductor ripple current at the same level. In contrast, the integrated circuit can operate with relatively small inductance because the voltage applied to L_X is significantly reduced.
- In the integrated circuit, the power decoupling circuit is connected in series with the

GCC circuit, and so the charging and discharging power to C_X passes through the GCC circuit. Because of this relationship, losses due to charging and discharging power occur in the inductor and switches in the GCC. In the individual circuit, the charging/discharging power is transmitted directly from the DC bus to the C_X, so the loss due to charging/discharging power is only in the power decoupling circuit.

From the above three points, it can be seen that both integrated and individual circuits have advantages and disadvantages. In addition to these circuit configurations, it is necessary to clarify the circuit configuration suitable for PV systems by examining the control characteristics.

4.1.2 Operation principle of GCC

The total voltage of each PV module is determined by the average DC voltage V_{DC} and is expressed in (4.1).

$$V_1 + V_2 + V_3 = V_{DC} \tag{4.1}$$

Each PV voltage in a buck-boost converter section is expressed in (4.2) using the off-duty ratio $\overline{D}$ of the buck-boost converter.

$$\begin{aligned} V_1 : V_2 : V_3 : V_X &= 1 : \frac{\overline{D}_{12}}{\overline{D}_{11}} : \frac{\overline{D}_{12}}{\overline{D}_{11}}\frac{\overline{D}_{22}}{\overline{D}_{22}} : \frac{\overline{D}_{12}}{\overline{D}_{11}}\frac{\overline{D}_{22}}{\overline{D}_{21}}\frac{\overline{D}_{X2}}{\overline{D}_{X1}} \\ &= 1 : k_1 : k_1k_2 : k_1k_2k_X \end{aligned} \tag{4.2}$$

From Eqs. (4.1) and (4.2), it can be observed that GCC adjusts each PV voltage to the maximum operating voltage through V_{DC} and $\overline{D}$. Therefore, all the PV modules can produce their maximum power, and the generation characteristics of the PV array have only one peak power point, and the influence on the MPPT control can be suppressed.

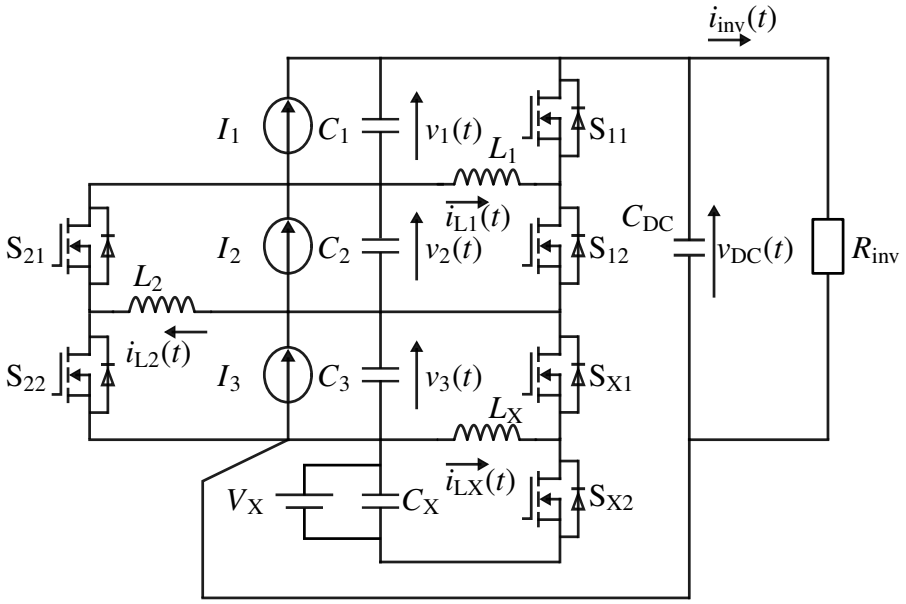


Figure 4.3. Equivalent circuit of integrated circuit.

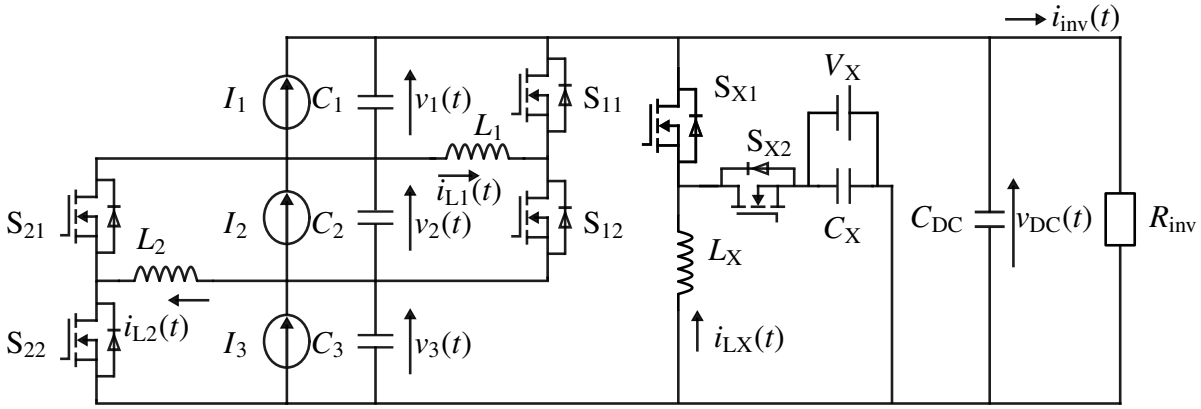


Figure 4.4. Equivalent circuit of individual circuit.

4.2 Analysis of PV system with active power decoupling and generation control features

4.2.1 Analysis of integrated and individual circuit

The integrated and individual circuits were analyzed using the state-space averaging method. Figs. 4.3 and 4.4 show the target circuits to be analyzed, wherein the inverter circuit is replaced by a resistor R_{inv}. Table 4.2 shows the conditions considered in the analysis and Table 4.3 summarizes variable definitions. PV module currents I_1–I_3 and

Table 4.2. Analysis conditions.

Parameter	Value
Equivalent resistance R_{inv}	44.1 Ω
parasitic resistance r_{L1},r_{L2} of L_1,L_2	10 mΩ
parasitic resistance r_{LX} of L_{LX}	69.5 mΩ
On resistance r_{S}	72 mΩ
PV equivalent current I_1	3.5 A
PV equivalent current I_2	5 A
PV equivalent current I_3	5.5 A

Table 4.3. variable definitions.

S_{11} :D_1,S_{12}:$\overline{D}_1$	$\overline{D}_{\mathrm{n}}$=1-$D_{\mathrm{n}}$
S_{21} :D_2,S_{22}:$\overline{D}_2$	C_1=C_2=C_3=C
S_{X1} :D_{X},S_{X2}:$\overline{D}_{\mathrm{X}}$	C_{DC}=aC

Table 4.4. Switching combinations.

Pattern	S_{11}	S_{12}	S_{21}	S_{22}
1	ON	OFF	ON	OFF
2	OFF	ON	ON	OFF
3	ON	OFF	OFF	ON
4	OFF	ON	OFF	ON

decoupling capacitor voltage V_{X} are assumed to be constant, represented by the constant current and voltage sources, respectively. The state vectors $x(t)$ and y are defined as in (4.3) and (4.4).

$$x(t) = [i_{\mathrm{L1}}(t), i_{\mathrm{L2}}(t), i_{\mathrm{LX}}(t), v_1(t), v_2(t), v_3(t)] \tag{4.3}$$

$$y = [I_1, I_2, I_3, V_{\mathrm{X}}] \tag{4.4}$$

The state-space averaging equation is expressed in (4.5).

$$\frac{d\overline{x}(t)}{dt} = A\overline{x}(t) + By \tag{4.5}$$

In the integrated and individual circuits, the duty ratio of each switch must be considered, as six switches are used. However, if all switches are considered simultaneously, the

equation becomes complicated. Therefore, the switching states of S_{11}–S_{22} are assumed to be fixed values, and the state-space averaged equation is derived with the duty ratio of switches S_{X1} and S_{X2}, which are assumed to be variables. There are four patterns of the switching combinations, as shown in Table 3. Comparing each pattern of the coefficient matrices A and B, the matrix in (4.6)–(4.8) that uses the duty ratio of all switches is derived.

$$
\begin{aligned}
A_{\text{integrated}} &= D_1 D_2 A^1 + \overline{D}_1 D_2 A^2 + D_1 \overline{D}_2 A^3 + \overline{D}_1 \overline{D}_2 A^4 \\
&= \begin{bmatrix}
-\frac{r_1}{L_1} & 0 & 0 & \frac{D_1}{L_1} & -\frac{\overline{D}_1}{L_1} & 0 \\
0 & -\frac{r_2}{L_2} & 0 & 0 & \frac{D_2}{L_2} & -\frac{\overline{D}_2}{L_2} \\
0 & 0 & -\frac{r_X}{L_X} & 0 & 0 & \frac{D_X}{L_X} \\
O_1 & P_2 & \frac{ma\overline{D}_X}{C} & -\frac{m}{R_{\text{inv}}C} & -\frac{m}{R_{\text{inv}}C} & -\frac{m}{R_{\text{inv}}C} \\
Q_1 & O_1 & \frac{ma\overline{D}_X}{C} & -\frac{m}{R_{\text{inv}}C} & -\frac{m}{R_{\text{inv}}C} & -\frac{m}{R_{\text{inv}}C} \\
P_1 & Q_2 & \frac{\overline{D}_X}{C}(ma-1) & -\frac{m}{R_{\text{inv}}C} & -\frac{m}{R_{\text{inv}}C} & -\frac{m}{R_{\text{inv}}C}
\end{bmatrix}
\end{aligned}
\tag{4.6}
$$

$$
\begin{aligned}
A_{\text{individual}} &= D_1 D_2 A^1 + \overline{D}_1 D_2 A^2 + D_1 \overline{D}_2 A^3 + \overline{D}_1 \overline{D}_2 A^4 \\
&= \begin{bmatrix}
-\frac{r_1}{L_1} & 0 & 0 & \frac{D_1}{L_1} & -\frac{\overline{D}_1}{L_1} & 0 \\
0 & -\frac{r_2}{L_2} & 0 & 0 & \frac{D_2}{L_2} & -\frac{\overline{D}_2}{L_2} \\
0 & 0 & -\frac{r_X}{L_X} & \frac{D_X}{L_X} & \frac{D_X}{L_X} & \frac{D_X}{L_X} \\
O_1 & P_2 & \frac{D_X}{C}(\frac{ma}{3}-1) & -\frac{m}{R_{\text{inv}}C} & -\frac{m}{R_{\text{inv}}C} & -\frac{m}{R_{\text{inv}}C} \\
Q_1 & O_1 & \frac{D_X}{C}(\frac{ma}{3}-1) & -\frac{m}{R_{\text{inv}}C} & -\frac{m}{R_{\text{inv}}C} & -\frac{m}{R_{\text{inv}}C} \\
P_1 & Q_2 & \frac{D_X}{C}(\frac{ma}{3}-1) & -\frac{m}{R_{\text{inv}}C} & -\frac{m}{R_{\text{inv}}C} & -\frac{m}{R_{\text{inv}}C}
\end{bmatrix}
\end{aligned}
\tag{4.7}
$$

$$
\begin{aligned}
B &= D_1 D_2 B^1 + \overline{D}_1 D_2 B^2 + D_1 \overline{D}_2 B^3 + \overline{D}_1 \overline{D}_2 B^4 \\
&= \begin{bmatrix}
0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 \\
0 & 0 & 0 & -\frac{\overline{D}_X}{L_X} \\
\frac{1}{C}(1-ma) & \frac{ma}{C} & -\frac{ma}{C} & 0 \\
\frac{ma}{C} & \frac{1}{C}(1-ma) & -\frac{ma}{C} & 0 \\
\frac{ma}{C} & -\frac{ma}{C} & \frac{1}{C}(1-ma) & 0
\end{bmatrix}
\end{aligned} \tag{4.8}
$$

Variables O_n, P_n, and Q_n are expressed in Eqs. (4.9)–(4.11)

$$O_n = -\frac{1}{C}\{D_n(1-2ma) + ma\} \tag{4.9}$$

$$P_n = \frac{1}{C} ma\{2D_n - 1\} \tag{4.10}$$

$$Q_n = -\frac{1}{C}\{D_n(1-2ma) + ma - 1\} \tag{4.11}$$

Variables r_1, r_2, r_X, and m are expressed in (4.12)–(4.14).

$$r_X = r_{LX} + D_n r_{Sn1} + \overline{D}_n r_{Sn2} (n = 1, 2) \tag{4.12}$$

$$r_X = r_{LX} + D_X r_{SX1} + \overline{D}_X r_{SX2} \tag{4.13}$$

$$m = \frac{C_1 C_2 C_3}{(C_1 C_2 + C_1 C_3 + C_2 C_3) C_{DC} + C_1 C_2 C_3} = \frac{1}{1+3a} \tag{4.14}$$

The matrix B is identical to each circuit configuration. Regarding the matrix A in the integrated circuit, the voltages V_1 and V_2 are not related to i_{LX}. However, in the individual circuit, since the APD section is connected to the DC input port, it is understood.

4.2.2 Derivation of disturbance suppression characteristic of APD control

If the fluctuation of the inverter input current $\Delta I_{\mathrm{inv}}(s)$ is given as a disturbance, the disturbance suppression characteristic of $\Delta V_{\mathrm{DC}}(s)$ at a target frequency of 100 Hz is derived when the APD control operates. Here, the integrated circuit is analyzed. First, the plant model of the integrated circuit is derived. The response of $\Delta X(s)$ to the fluctuations $\Delta V_{\mathrm{X}}(s)$, $\Delta R_{\mathrm{inv}}(s)$, and $\Delta D_{\mathrm{X}}(s)$ is expressed in (4.15), which is derived from Eqs. (4.5), (4.6), and (4.8).

$$\begin{aligned}(s-A)\Delta X(s) = B_4\Delta V_{\mathrm{X}}(s) + \frac{\partial A}{\partial R_{\mathrm{inv}}}X\Delta R_{\mathrm{inv}}(s) \\ + (\frac{\partial A}{\partial D_{\mathrm{X}}}X + \frac{\partial B}{\partial D_{\mathrm{X}}}Y)\Delta D_{\mathrm{X}}(s)\end{aligned} \tag{4.15}$$

Here, the fluctuations in I_1–I_3 are ignored and B_4 represents the fourth row of (4.8). Eq. (4.15) is rearranged for $\Delta X(s)$, and $\Delta X(s)$ is expressed in Eq. (4.16) as the sum of $\Delta I_{\mathrm{inv}}(s)$ and $\Delta D_{\mathrm{X}}(s)$.

$$\begin{aligned}\Delta X(s) &= (sE - A - F - G)^{-1}\{-\frac{R_{\mathrm{inv}}^2}{V_{\mathrm{DC}}}\frac{\partial A}{\partial R_{\mathrm{inv}}}X\Delta I_{\mathrm{inv}}(s) \\ &\quad + (\frac{\partial A}{\partial D_{\mathrm{X}}}X + \frac{\partial B}{\partial D_{\mathrm{X}}}Y)\Delta D_{\mathrm{X}}(s)\} \\ &= X_{\mathrm{inv}}\Delta I_{\mathrm{inv}}(s) + X_{\mathrm{DX}}\Delta D_{\mathrm{X}}(s) \\ &= \left[\frac{\Delta I_{\mathrm{L1}}(s)}{\Delta I_{\mathrm{inv}}(s)} \quad \frac{I_{\mathrm{L2}}(s)}{\Delta I_{\mathrm{inv}}(s)} \quad \frac{I_{\mathrm{LX}}(s)}{\Delta I_{\mathrm{inv}}(s)} \quad \frac{\Delta V_1(s)}{\Delta I_{\mathrm{inv}}(s)} \quad \frac{\Delta V_2(s)}{\Delta I_{\mathrm{inv}}(s)} \quad \frac{\Delta V_3(s)}{\Delta I_{\mathrm{inv}}(s)}\right]\Delta I_{\mathrm{inv}}(s) \\ &\quad + \left[\frac{\Delta I_{\mathrm{L1}}(s)}{\Delta D_{\mathrm{X}}(s))} \quad \frac{I_{\mathrm{L2}}(s)}{\Delta D_{\mathrm{X}}(s)} \quad \frac{I_{\mathrm{LX}}(s)}{\Delta D_{\mathrm{X}}(s)} \quad \frac{\Delta V_1(s)}{\Delta D_{\mathrm{X}}(s)} \quad \frac{\Delta V_2(s)}{\Delta D_{\mathrm{X}}(s)} \quad \frac{\Delta V_3(s)}{\Delta D_{\mathrm{X}}(s)}\right]\Delta D_{\mathrm{X}}(s) \\ &= \left[\Delta I_{\mathrm{L1inv}}(s) \quad \Delta I_{\mathrm{L2inv}}(s) \quad \Delta I_{\mathrm{LXinv}}(s) \quad \Delta V_{\mathrm{1inv}}(s) \quad V_{\mathrm{2inv}}(s) \quad V_{\mathrm{3inv}}(s)\right]\Delta I_{\mathrm{inv}}(s) \\ &\quad + \left[\Delta I_{\mathrm{L1DX}}(s) \quad \Delta I_{\mathrm{L2DX}}(s) \quad \Delta I_{\mathrm{LXDX}}(s) \quad \Delta V_{\mathrm{1DX}}(s) \quad V_{\mathrm{2DX}}(s) \quad V_{\mathrm{3DX}}(s)\right]\Delta D_{\mathrm{X}}(s)\end{aligned} \tag{4.16}$$

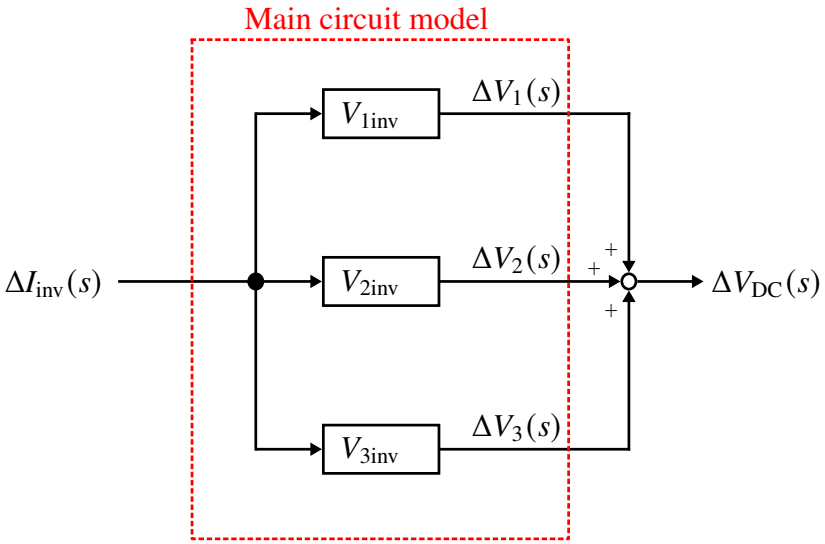


Figure 4.5. Block diagram without APD control.

where E represents the identity matrix and the coefficient matrices F and G are calculated from $\Delta V_{\mathrm{X}}(s)$ and $\Delta R_{\mathrm{inv}}(s)$, as shown in (4.17) and (4.18), respectively.

$$\Delta V_{\mathrm{X}}(s) = \frac{\overline{D}_{\mathrm{X}}}{sC_{\mathrm{X}}}\Delta I_{\mathrm{LX}} = \frac{1}{s}\begin{bmatrix}0 & 0 & \frac{\overline{D}_{\mathrm{X}}}{C_{\mathrm{X}}} & 0 & 0 & 0\end{bmatrix}\Delta X(s) \tag{4.17}$$

$$\begin{aligned}\Delta R_{\mathrm{inv}}(s) &= -\frac{R_{\mathrm{inv}}^2}{V_{\mathrm{DC}}}\Delta I_{\mathrm{inv}} + \frac{R_{\mathrm{inv}}}{V_{\mathrm{DC}}}(\Delta V_1 + \Delta V_2 + \Delta V_3) \\ &= -\frac{R_{\mathrm{inv}}^2}{V_{\mathrm{DC}}}\Delta I_{\mathrm{inv}} + \frac{R_{\mathrm{inv}}}{V_{\mathrm{DC}}}\begin{bmatrix}0 & 0 & 0 & 1 & 1 & 1\end{bmatrix}\Delta X(s)\end{aligned} \tag{4.18}$$

that each PV voltage has an effect on i_{LX}. In addition, $\Delta V_{\mathrm{DC}}(s)$ is expressed in (4.19) as the sum of the fluctuations of the PV voltages $\Delta V_1(s)$, $\Delta V_2(s)$, and $\Delta V_3(s)$.

$$\begin{aligned}\Delta V_{\mathrm{DC}}(s) &= \Delta V_1 + \Delta V_2 + \Delta V_3 \\ &= (V_{1\mathrm{inv}} + V_{2\mathrm{inv}} + V_{3\mathrm{inv}})\Delta I_{\mathrm{inv}}(s) + (V_{1\mathrm{DX}} + V_{2\mathrm{DX}} + V_{3\mathrm{DX}})\Delta D_{\mathrm{X}}(s)\end{aligned} \tag{4.19}$$

The plant model of the proposed circuit is expressed in (4.16) and (4.19).

Next, the fluctuation of the input voltage $\Delta V_{\mathrm{DC}}(s)$ with and without APD control is

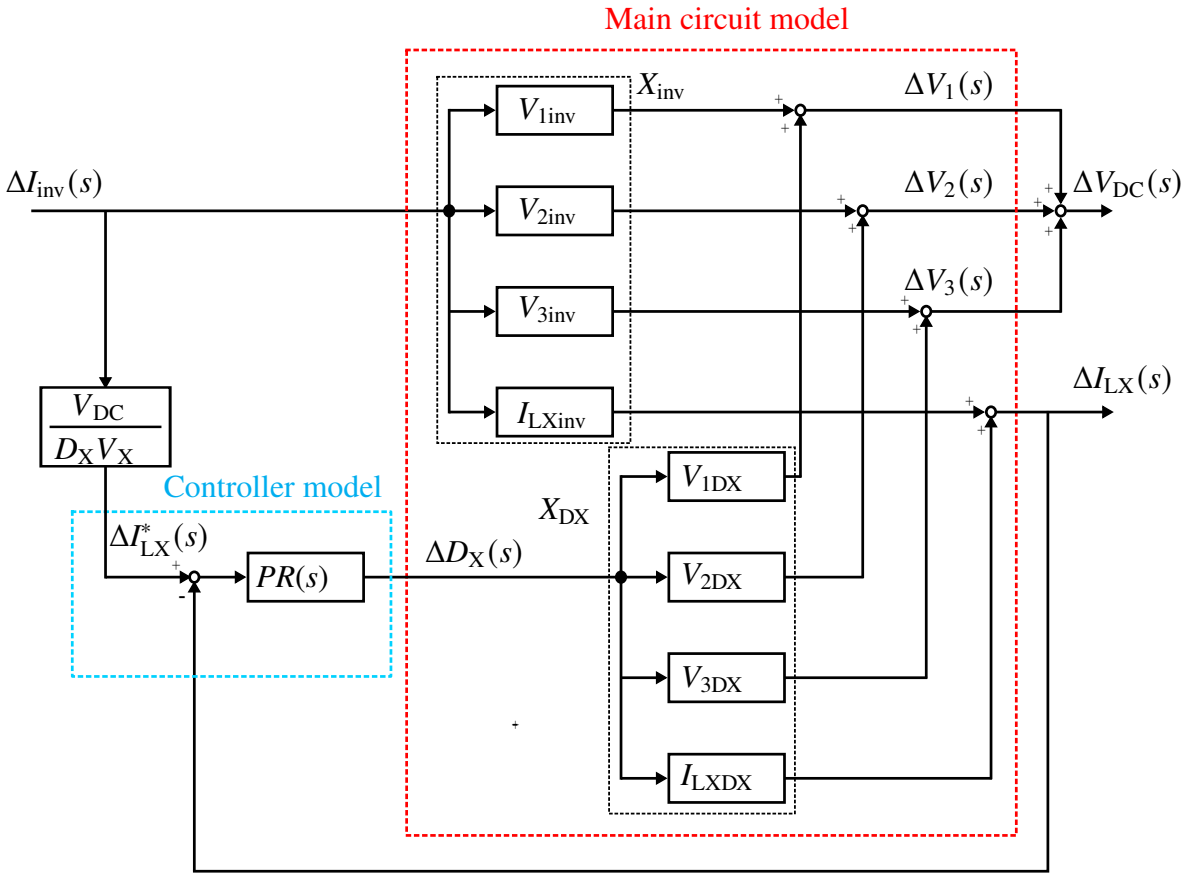


Figure 4.6. Block diagram with APD control.

derived from (4.16) and (4.19). Fig. 4.5 shows the block diagram of the plant model without APD control. Without APD control, $\Delta D_X(s)$ has no fluctuation and $\Delta V_{DC}(s)$ is determined only by $\Delta I_{inv}(s)$. $\Delta V_{DC}(s)$ without APD control is expressed in (4.20).

$$\Delta V_{DC}(s) = (V_{1inv} + V_{2inv} + V_{3inv})\Delta I_{inv}(s) \tag{4.20}$$

Fig. 4.6 shows the block diagram of the plant model with the APD control model. The fluctuation of the input voltage with APD control $\Delta V_{DCAPD}(s)$ is determined by $\Delta I_{inv}(s)$ and $\Delta D_X(s)$. The quantity $\Delta I_{LXAPD}(s)$ for the feedback loop is expressed by $\Delta I_{inv}(s)$ as shown in (4.21).

$$\begin{aligned}\Delta I_{LXAPD}(s) &= \frac{1}{1 + PR(s) * I_{LXDX}}\{-PR(s)\frac{V_{DC}}{D_X V_X} * I_{LXDX} + I_{LXinv}\}\Delta I_{inv(s)} \\ &= I_{LXAPD}\Delta I_{inv}(s)\end{aligned} \tag{4.21}$$

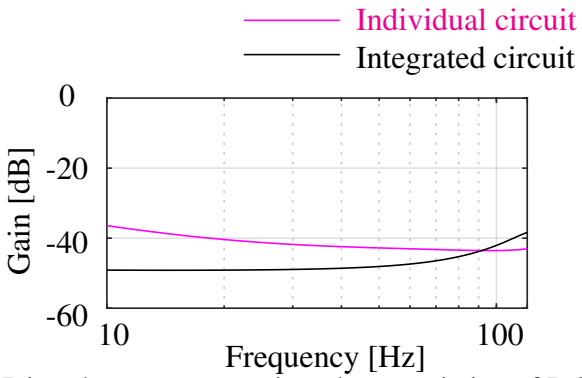


Figure 4.7. Disturbance suppression characteristics of DC voltage V_{DC}.

From Fig. 4.6 and (4.21), the fluctuation of the PV voltage with APD control $\Delta V_{\mathrm{nAPD}}(s)$, is expressed in (4.22).

$$\begin{aligned}\Delta V_{\mathrm{nAPD}}(s) &= \{-PR(s)\frac{V_{\mathrm{DC}}}{D_{\mathrm{X}}V_{\mathrm{X}}} * I_{\mathrm{LXAPD}}V_{\mathrm{nDX}} + V_{\mathrm{ninv}}\}\Delta I_{\mathrm{inv}(s)} \\ &= V_{\mathrm{nAPD}}\Delta I_{\mathrm{inv}}(s)\ (n = 1-3)\end{aligned} \tag{4.22}$$

The disturbance suppression characteristic of $\Delta V_{\mathrm{DC}}(s)$ for the APD control is derived by dividing $\Delta V_{\mathrm{DCAPD}}(s)$ and $\Delta V_{\mathrm{DC}}(s)$ without APD control. From (4.20) and (4.22), the disturbance suppression characteristic is expressed by (4.23).

$$\frac{\Delta V_{\mathrm{DCAPD}}(s)}{\Delta V_{\mathrm{DC}}(s)} = \frac{(V_{1\mathrm{APD}} + V_{2\mathrm{APD}} + V_{3\mathrm{APD}})\Delta I_{\mathrm{inv}}(s)}{(V_{1\mathrm{inv}} + V_{2\mathrm{inv}} + V_{3\mathrm{inv}})\Delta I_{\mathrm{inv}}(s)} \tag{4.23}$$

Additionally, the disturbance suppression characteristics of the conventional circuit are derived by substituting (4.6) into (4.7), and a procedure similar to the previous calculation is used.

4.2.3 Evaluation of the disturbance suppression characteristic of APD control

Fig. 4.7 shows the disturbance suppression characteristic of V_{DC} in terms of both configurations. It has been confirmed that the integrated circuit can suppress not only the target frequency (at 100 Hz) but also an integral multiple frequencies of 100 Hz by using APD

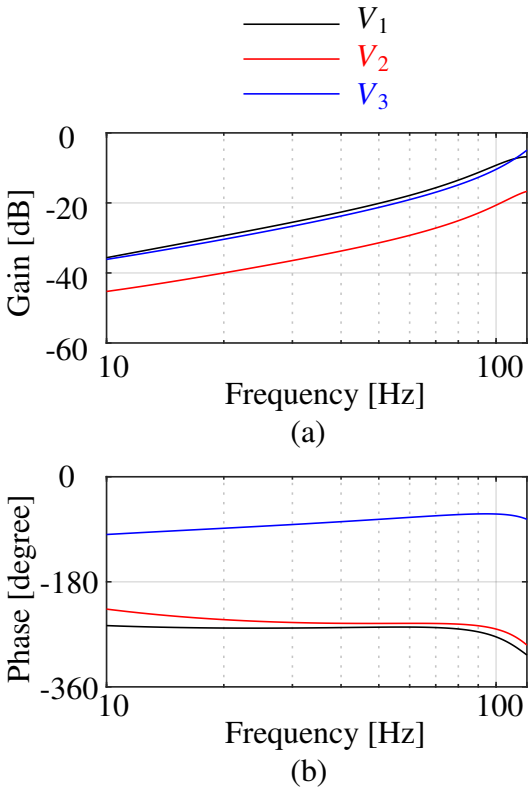


Figure 4.8. Disturbance suppression characteristics of PV voltage in integrated circuit. (a) Gain-frequency characteristics. (b) Phase-frequency characteristics.

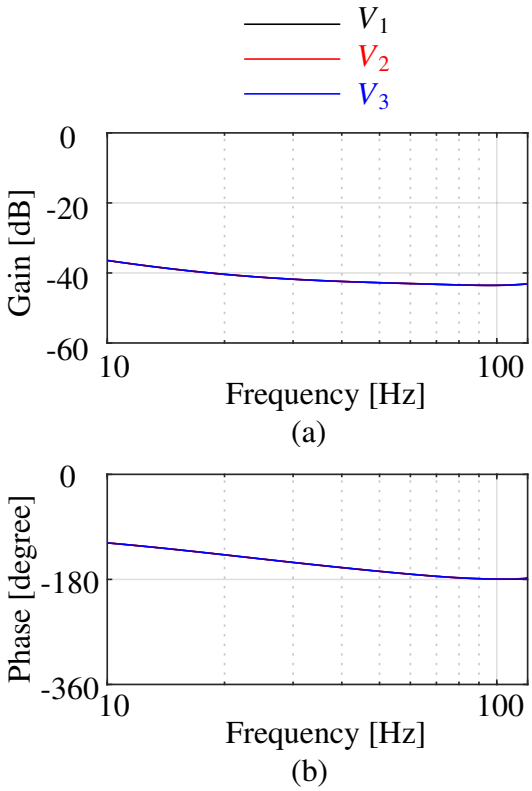


Figure 4.9. Disturbance suppression characteristics of PV voltage in individual circuit. (a) Gain-frequency characteristics. (b) Phase-frequency characteristics.

control. Conversely, the individual circuit can suppress 100 Hz, which is very similar to the proposed circuit, but the suppression effect of the conventional circuit is significantly reduced at 200 and 300 Hz compared to that of the integrated circuit. Figs. 4.8 and 4.9 show the disturbance suppression characteristics of the PV voltage for each configuration derived from (4.24).

$$\frac{\Delta V_{\mathrm{nAPD}}(s)}{\Delta V_{\mathrm{n}}(s)} = \frac{V_{\mathrm{nAPD}}\Delta I_{\mathrm{inv}}(s)}{V_{\mathrm{ninv}}\Delta I_{\mathrm{inv}}(s)} \ (n = 1 - 3) \tag{4.24}$$

In the integrated circuit, the frequency characteristics of each PV module tend to be similar; however, there is a difference in the suppression effect of each PV voltage. Each PV module produces power depending on its output voltage. If a fluctuation appears in

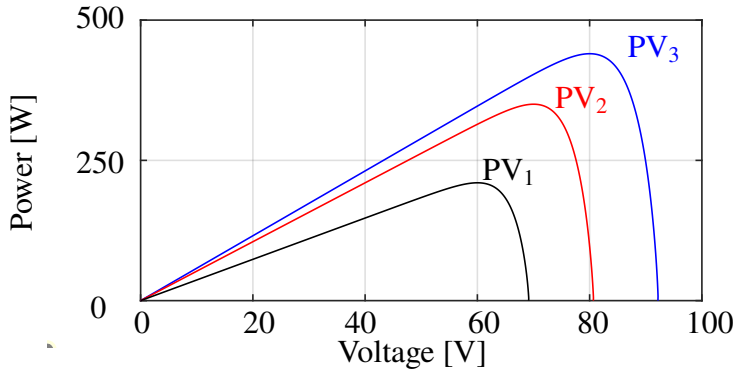


Figure 4.10. PV characteristics for real-time simulation.

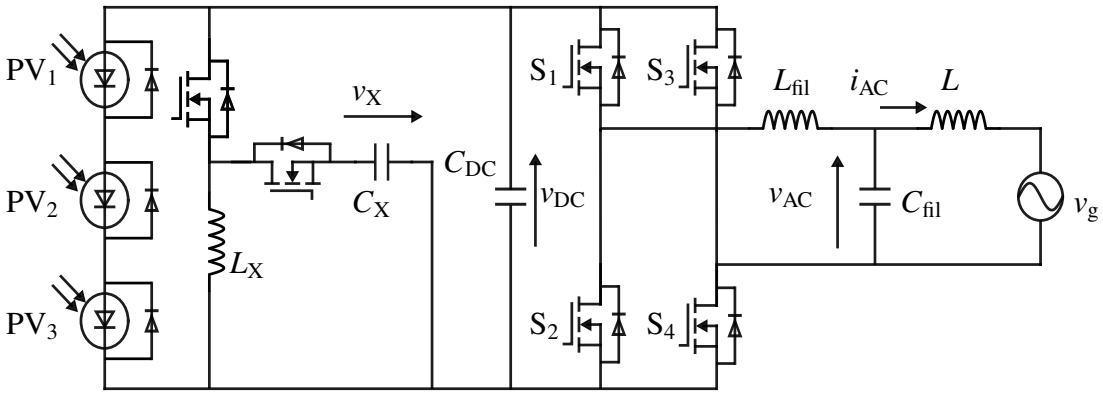


Figure 4.11. Main circuit configuration of APD circuit with partial shade.

the PV voltage, the operating point moves away from the optimal point; thus, the average generated power decreases compared to the maximum power, and the power generation efficiency also declines. From the above characteristics, there is a possibility that the proposed circuit cannot fully utilize the potential generated power of PV_1 and PV_3 with respect to PV_2. In addition, the individual circuit shows similar frequency characteristics between each PV module in a low frequency band up to around 100 Hz.

4.3 Verification result

The validity of the characteristics of the APD control was analyzed and verified by using real-time simulation. Fig. 4.10 shows the PV characteristics used in this verification. The power generation characteristics of each PV are changed assuming the case that the PV array is in partial shade. Fig. 4.11 shows a circuit configuration assuming the case

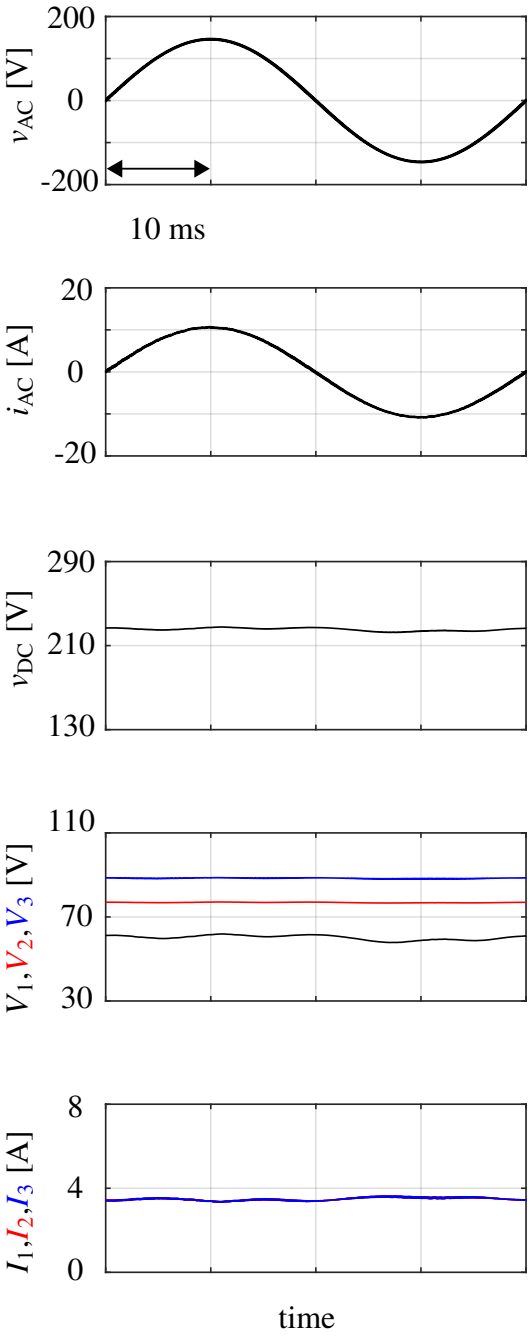


Figure 4.12. Operation waveforms of conventional APD circuit.

of partial shading in a conventional APD circuit. In the integrated circuit, there is a difference between the disturbance suppression characteristics of the PV voltages; hence, it is estimated that the average generated power decreases from the maximum power. Therefore, in this verification, the power generation efficiency of PV η_{PVn} is defined by

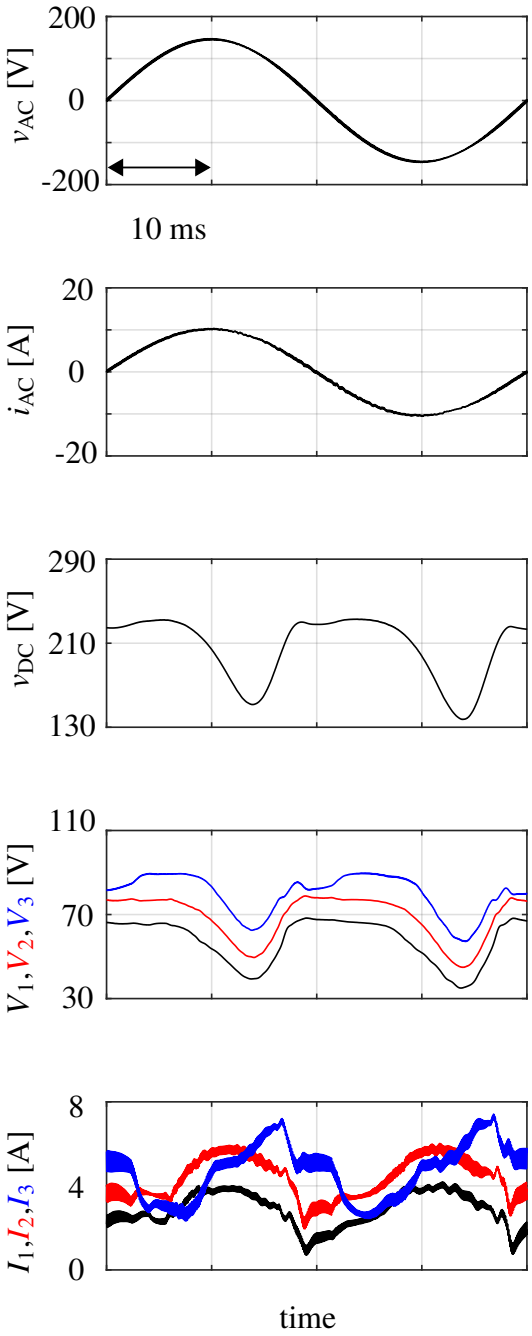


Figure 4.13. Operation waveforms without APD control of integrated circuit.

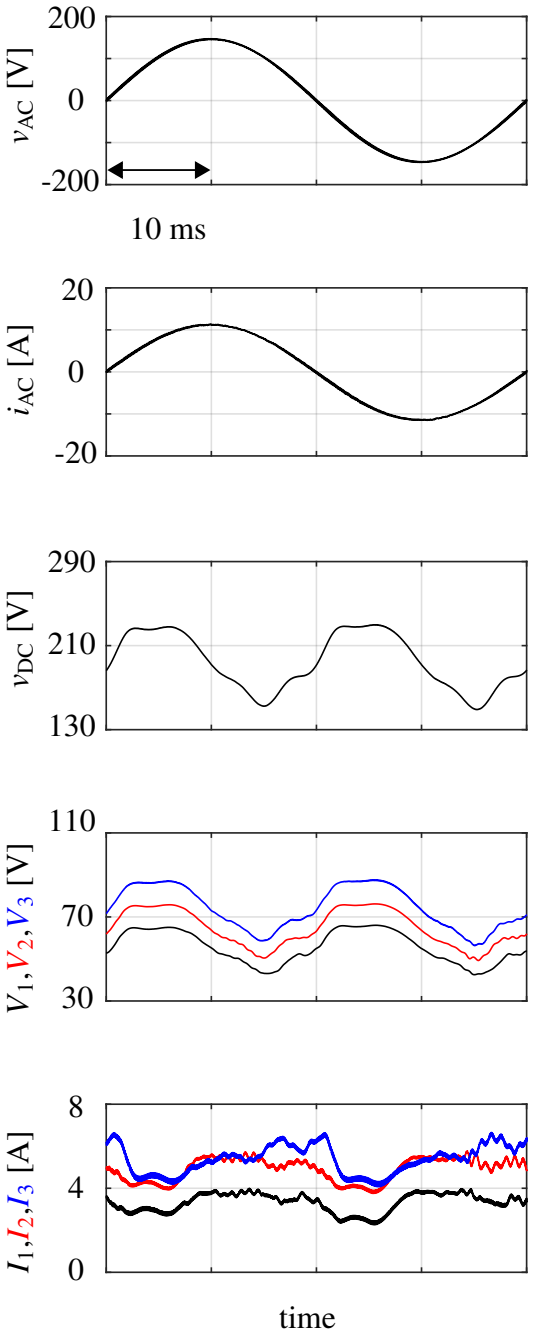


Figure 4.14. Operation waveforms without APD control of individual circuit.

(4.25) and is also evaluated for each PV module.

$$\eta_{\mathrm{PVn}} = \frac{P_{\mathrm{PVn}}}{P_{\mathrm{PVnmax}}} = \frac{I_{\mathrm{n}} V_{\mathrm{n}}}{P_{\mathrm{PVnmax}}} \tag{4.25}$$

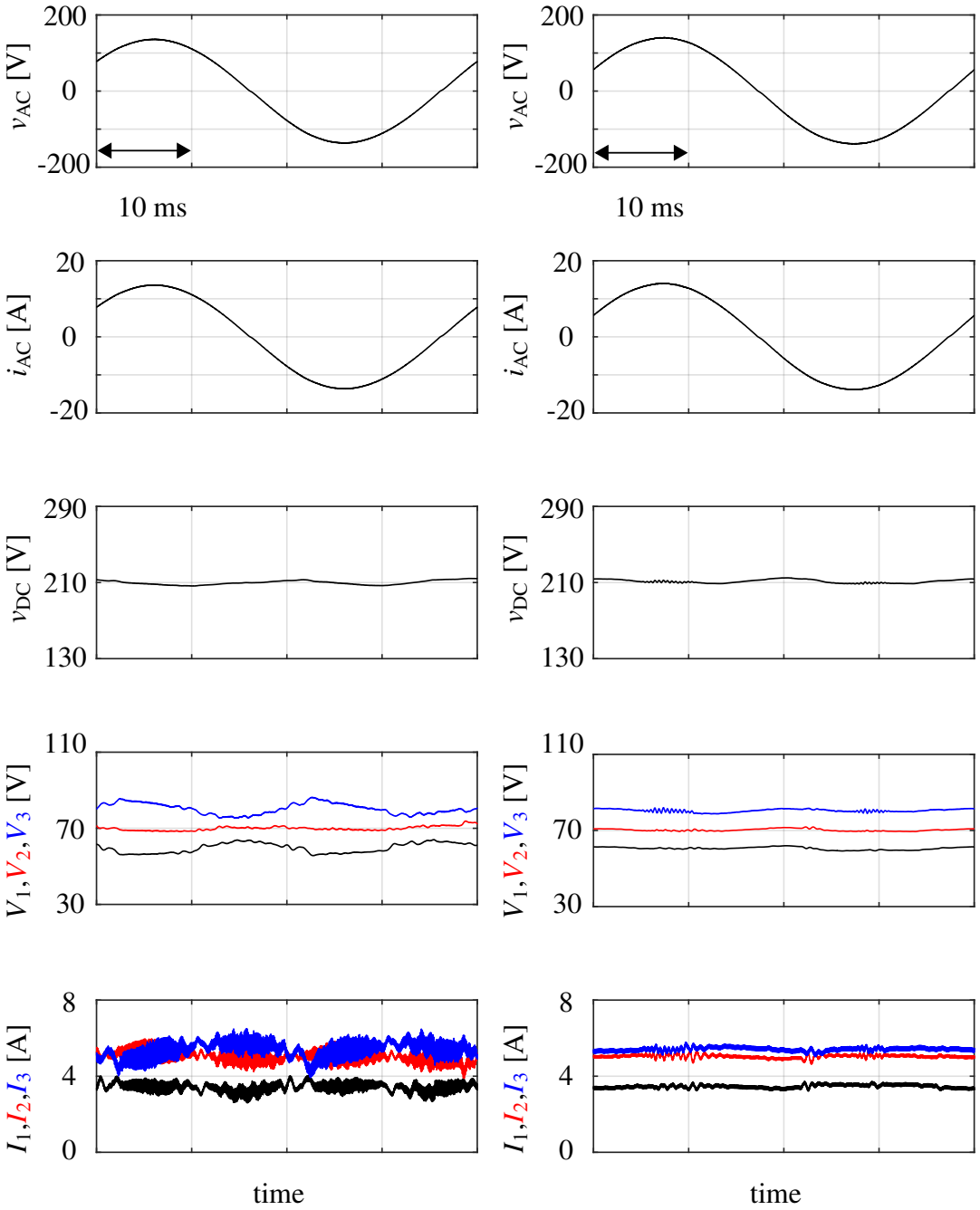


Figure 4.15. Operation waveforms with APD control of integrated circuit.

Figure 4.16. Operation waveforms with APD control of individual circuit.

Here, P_{PVnmax} is defined as the maximum generated power of the PV module and P_{PVn} is defined as the average output power of the PV module, which is derived from the average value of the PV voltage V_{n} and the average value of the PV current I_{n}.

Fig. 4.12 shows the operating waveforms of the APD circuit when partial shade occurs.

Table 4.5. Evaluation of PV power generation efficiency.

	Maximum power	Conventional APD	Integrated circuit	Individual circuit
PV_1	210 W	209.6 W(99.8%)	204.1 W(97.2%)	208.9 W(99.5%)
PV_2	350 W	267.8 W(76.5%)	348.1 W(99.5%)	348.9 W(99.7%)
PV_3	450 W	308.4 W(70.1%)	430.3 W(97.8%)	437.4 W(99.4%)
Total	1000 W	785.8 W (78.6%)	982.5 W(98.3%)	995.2 W(99.5%)

The waveforms show the inverter output voltage v_{AC}, inverter current i_{AC}, DC voltage v_{DC}, PV voltages V_1, V_2, V_3, and PV currents I_1, I_2, I_3 from the top. A low-pass filter (LPF) is applied to each waveform to remove the switching frequency components. It can be confirmed from the PV current waveforms that the operating voltage of each PV is determined by the current and that the maximum power of each PV is not produced.

Figs. 4.13 and 4.14 show the operating waveform without APD control in integrated and individual circuits. For v_{DC} waveform, it is confirmed that the ripple voltage of v_{DC} appears with 46 $V_{p\text{-}p}$(Integrated circuit) and 44 $V_{p\text{-}p}$(Individual circuit).

Figs. 4.15 and 4.16 show the operating waveform with APD control in integrated and individual circuits. Here, because of the calculation speed of the microcontroller, 10 Ω resistive load is used instead of grid voltage v_g, and the inverter is controlled by open-loop control. For v_{AC} and i_{AC}, both circuits produce AC wave, and it can be confirmed that the APD control does not affect the inverter control and the power pulsation can be stored in the decoupling capacitor by charging and discharging actions. Comparing the THD of i_{AC} in both circuits, the distortion in the individual circuit was 0.91% and 0.87% in the integrated circuit; the THD of the integrated circuit is evidently lower than that of the individual circuit. This can be attributed to the high-frequency components contained in v_{DC} that are transmitted to the output, when the individual circuit is used.

For v_{DC} waveform, the ripple voltage of v_{DC} is reduced to 6 $V_{p\text{-}p}$ (individual circuit) and to 7 $V_{p\text{-}p}$ (integrated circuit). For PV voltage, it is confirmed that the average voltage of each PV module is maintained at an optimum voltage by the GCC in both circuits. As shown in the analysis, each PV voltage is imbalanced when the integrated circuit

is used. This is because switches S_{X1} and S_{X2} in the APD section use the feedback loop to control the inductor current, while switches S_{11}–S_{22} in the GCC section are in an open loop. Meanwhile, in the individual circuit, there is no difference in amplitude between the PV voltages, and each PV module has the same suppression effect. It can be confirmed that high-frequency components are generated on each PV voltage as well. The PV power generation efficiency is evaluated for both the circuits. Table 4.5 shows the calculation results using the average PV voltage and the average PV current derived from the simulation results. Because the maximum power of each PV cannot be output with the conventional APD circuit, the overall power generation efficiency is significantly reduced to 78.6%. It is clear from the table that the power generation efficiency of the individual circuit is 1.2% higher than that of the integrated circuit, because the amplitude of each PV voltage in the individual circuit is uniform and lower than that of the integrated circuit. Therefore, considering the power generation efficiency, it can be assumed that the individual circuit is more suitable for a PV system.

4.4 Summary

Chapter 4 described two configurations of PV inverters with GCC and APD features. Mathematical analysis was performed on both circuits using the state-space averaging method to clarify the dynamic characteristics of the APD control of both circuits. Furthermore, the disturbance suppression characteristics of the APD control were evaluated using dynamic characteristic analysis, and the differences in control characteristics depending on the configurations were outlined. The validity of the analysis was confirmed using a real-time simulation under an output power rating of 1 kVA and input voltage of 210 V. The operation of GCC suppressed partial shade and improved the power generation efficiency from 78.6% to 99.5%. In addition, the individual circuit was confirmed to be a more suitable circuit configuration for the PV system in view of its power generation efficiency.

Chapter 5

Active Power Decoupling Control Focusing on Harmonic Voltage

This chapter proposes the control strategies of APD for the compensation of power pulsation caused by both fundamental and harmonic components. Furthermore, the compensating power of the APD control is discussed when the grid voltage has the 3rd harmonic voltage. The influence of the 3rd harmonic voltage on the DC voltage ripple is evaluated. In the APD control, the power pulsation caused by the harmonic components is considered for compensating power calculation. The compensating power including the power pulsation caused by the fundamental and harmonic components is discussed based on the DC voltage ripple. The validity of APD control is verified on a 400 W inverter.

5.1 APD control considering harmonic voltage

5.1.1 Proposed compensating power calculation

Fig. 5.1 shows the main circuit configuration when harmonics are included, and Table 5.1 lists the circuit conditions; the APD circuit and LC filter parameters are those of Chapter 3.

Fig. 5.2 shows the compensating power calculation block of the APD control and Table 5.2 lists the control parameters. In the APD control, the compensating power command p_{X}^{*} is calculated from the sum of the power pulsation caused by the fundamental component

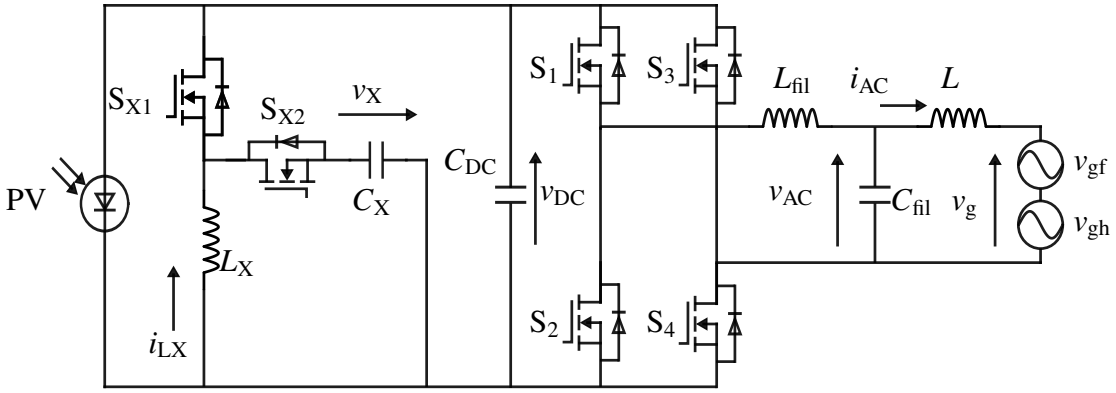
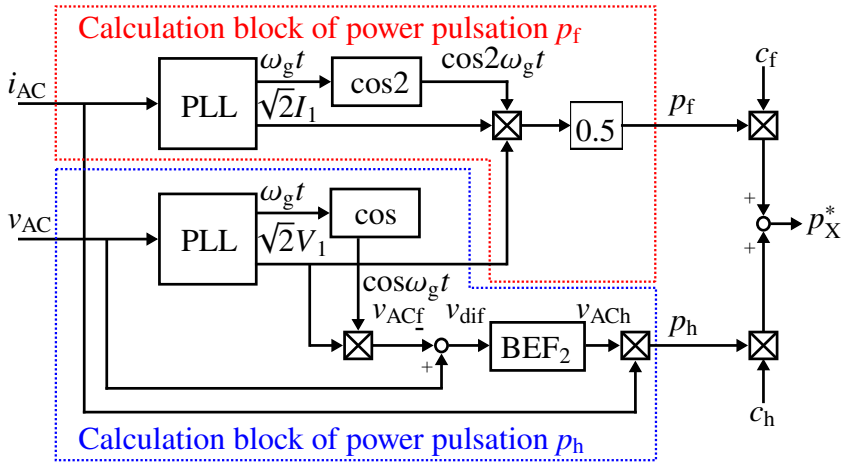


Figure 5.1. Main circuit configuration of APD circuit with harmonic voltage.

Table 5.1. Circuit parameters and specifications with harmonic component.

Parameter	Value
Average DC voltage V_{DC}	200 V
Output power p_{AC}	400 W
Grid voltage v_{gf}	100 V
3rd harmonic voltage v_{gh}	25 V (25%)
Grid frequency f_g	50 Hz
DC capacitance C_{DC}	50 µF



(a)

Figure 5.2. Compensating power calculation block of the APD control.

p_f and harmonic components p_h. Additionally, the compensation ratios c_f and c_h are used to control the 2nd and 4th power pulsations. The p_h is calculated from the output current i_{AC} and harmonic voltage v_{ACh}.

v_{ACh} is detected by removing the fundamental component using the difference waveform

Table 5.2. Control parameters of the APD control.

Parameter	Value
Resonant gain K_R	100
Proportional gain K_P	20
Resonant angular frequency ω_0	2*π*100 rad/s
Band angular frequency ω_b	2*π*10 rad/s
Eliminated angular frequency 1 ω_e1	2*π*100 rad/s
Band angular frequency 1 ω_b1	2*π*10 rad/s
Eliminated angular frequency 2 ω_e2	2*π*50 rad/s
Band angular frequency 2 ω_b2	2*π*10 rad/s

and BEF_2. The difference voltage v_dif is calculated from the output voltage v_AC and the fundamental voltage v_ACf is detected by PLL. The v_ACh can be detected regardless of the harmonic orders by suppressing the fundamental component only. The compensating power p_X is controlled using the control block in Fig. 3.2(b).

5.1.2 Evaluation of compensating power

The compensating power including the 2nd and 4th pulsation power is discussed based on the voltage ripple ratio α_VDCrip. Eq. (5.1) shows the voltage ripple ratio α_VDCrip, which is the ratio of the 2nd and 4th voltage ripple to V_DC.

$$\alpha_\mathrm{VDCrip} = \frac{\sqrt{\Delta v_\mathrm{DCrip2}^2 + \Delta v_\mathrm{DCrip4}^2}}{2V_\mathrm{DC}} \times 100 \tag{5.1}$$

The 2nd and 4th DC voltage ripples in the APD control are calculated as follows:

$$\Delta v_\mathrm{DCrip2} = \frac{(P_\mathrm{f} - P_\mathrm{h2}) - P_\mathrm{X2}}{\omega_\mathrm{g} V_\mathrm{DC} C_\mathrm{DC}} = \frac{(P_\mathrm{f} - P_\mathrm{h2}) - (c_\mathrm{f} P_\mathrm{f} - c_\mathrm{h} P_\mathrm{h2})}{\omega_\mathrm{g} V_\mathrm{DC} C_\mathrm{DC}}$$

$$\Delta v_\mathrm{DCrip4} = \frac{P_\mathrm{h4} - P_\mathrm{X4}}{2\omega_\mathrm{g} V_\mathrm{DC} C_\mathrm{DC}} = \frac{P_\mathrm{h4}(1 - c_\mathrm{h})}{2\omega_\mathrm{g} V_\mathrm{DC} C_\mathrm{DC}} \tag{5.2}$$

Because the APD control compensates for power pulsations caused by both the fundamental and harmonic components, the compensating power term is included in the DC voltage ripple of both the 2nd and 4th pulsations.

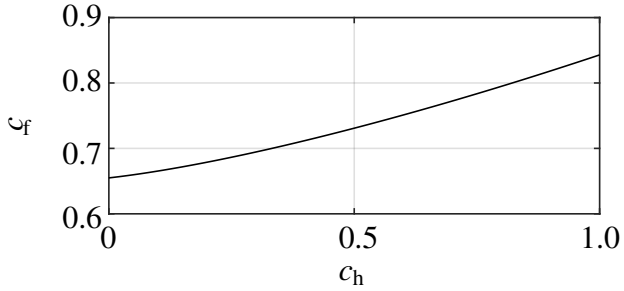


Figure 5.3. Relationship between compensation ratios c_f and c_h at voltage ripple ratio α_{VDCrip} = 5%.

Fig. 5.3 shows the compensation ratio of the power pulsation caused by fundamental component c_f that can achieve α_{VDCrip} of 5% for each compensation ratio of the power pulsation caused by harmonic component c_h in the analysis using (5.1) – (5.2) and Table 5.1. It can be confirmed that the compensation ratio c_f increases with an increase in the compensation ratio c_h.

Fig. 5.4 shows the relationship between compensating power ratio CP_{ratio} and c_h. Here, CP_{ratio} is defined as the ratio of the compensating power P_X to the output power pulsation P_{ripple} shown in (5.3). For lower CP_{ratio}, the power conversion loss of the APD circuit can be suppressed because the APD circuit operates with lower compensating power.

$$\begin{aligned} CP_{ratio} &= \frac{P_X}{P_{ripple}} \times 100 \\ &= \frac{\sqrt{(c_f P_f - c_h P_{h2})^2 + (c_h P_{h4})^2}}{\sqrt{(P_f - P_{h2})^2 + P_{h4}^2}} \times 100 \end{aligned} \tag{5.3}$$

The blue line represents CP_{ratio} using the combination of c_f and c_h shown in Fig. 5.3, and the blue point represents the minimum point of CP_{ratio} (c_f=0.73, c_h=0.51). The black point represents CP_{ratio} with 100% compensation for the 2nd and 4th power pulsations (c_f=1.0, c_h=1.0), whereas the red point represents CP_{ratio} with 100% compensation for only the 2nd power pulsation (c_f=0.75). The combination of the compensation ratios in Fig 5.3 can achieve lower power operation compared to the case with 100% compensation of the 2nd power pulsation and 100% compensation of the 2nd and 4th power pulsations.

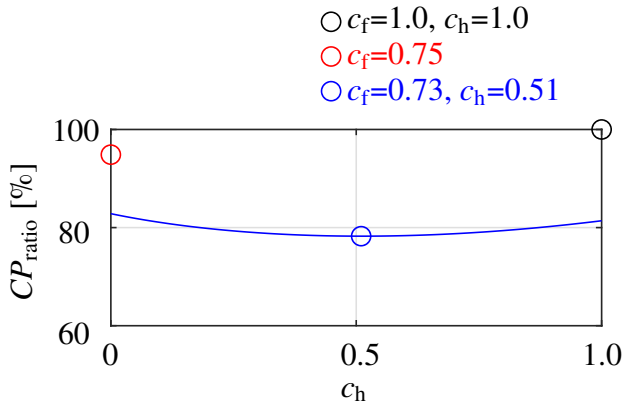


Figure 5.4. Relationship between compensating power ratio CP_{ratio} and compensation ratio c_{h}.

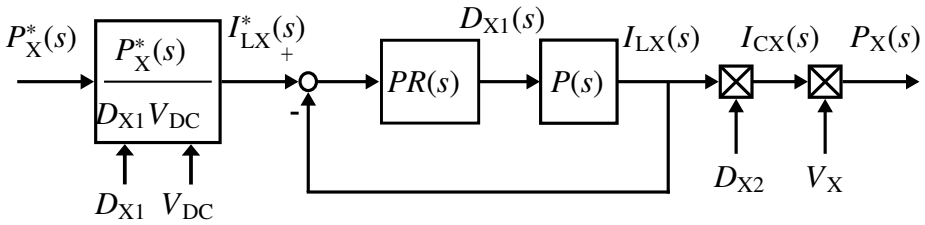


Figure 5.5. Block diagram of compensating power p_{X} control.

Additionally, the combination of compensation ratios c_{f} and c_{h} in Fig. 5.3 shows that the CP_{raito} is minimized by compensating 81% for the 2nd power pulsation and 51% for the 4th power pulsation.

5.1.3 Analysis of APD control

The APD control is required to be responsive to power pulsations of more than 100 Hz when the grid voltage has harmonic components. The response of the APD control was verified through the analysis of the compensating power p_{X} control. Fig. 5.5 shows the block diagram of the p_{X} control. The compensating power $P_{\text{X}}(s)$ is controlled by the inductor current $I_{\text{LX}}(s)$ to the inductor current command $I^*_{\text{LX}}(s)$. The duty ratio of switch S_{X1} $D_{\text{X1}}(s)$ is calculated by amplifying the deviation between $I^*_{\text{LX}}(s)$ and $I_{\text{LX}}(s)$ using the PR compensator $PR(s)$. $D_{\text{X1}}(s)$ is converted to $I_{\text{LX}}(s)$ through the plant model $P(s)$. The decoupling capacitor current $I_{\text{CX}}(s)$ is determined from the duty ratio of switch S_{X2} D_{X2} and $I_{\text{LX}}(s)$. The compensating power $P_{\text{X}}(s)$ is derived as the product of $I_{\text{CX}}(s)$ and the

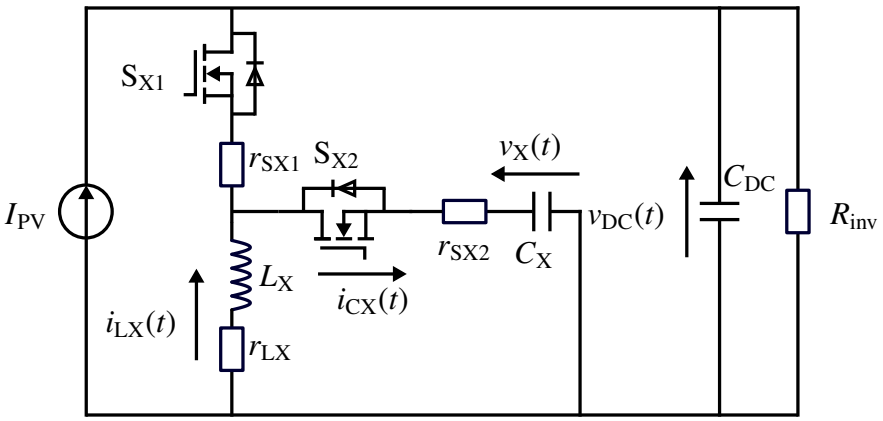


Figure 5.6. Equivalent circuit for analysis.

Table 5.3. Equivalent circuit parameters.

Parameter	Value
On-resistance r_{X1}, r_{X2}	72.0 mΩ
Parasitic resistance r_{LX}	69.5 mΩ
PV current I_{PV}	2 A
Equivalent resistance R_{inv}	100 Ω

average value of the decoupling capacitor voltage V_X. The transfer function $G_{PX}(s)$ is expressed as the response of $P_X(s)$ to the compensating power command $P_X^*(s)$ in (5.4).

$$G_{PX}(s) = \frac{P_X(s)}{P_X^*(s)} = \frac{D_{X2}V_X}{D_{X1}V_{DC}} \times \frac{P(s) \times PR(s)}{1 + P(s) \times PR(s)} \tag{5.4}$$

Fig. 5.6 shows the equivalent circuit for analysis and Table 5.3 lists the equivalent circuit parameters. The equivalent circuit in Fig. 5.6 uses a current source as input. The inverter is replaced by an equivalent resistance R_{inv}. Parasitic resistance r_{LX} is considered for inductor L_X and on-resistances r_{SX1} and r_{SX2} are considered for the switches S_{X1} and S_{X2}, respectively.

The plant model $P(s)$ was derived from the state-space averaging method [104]. Eq. (5.5) is the state-space averaged equation. Eq. (5.6) shows the coefficient matrix A. Eq. (5.7) shows the total resistance r_X. Here, $\overline{D}_{X1}$ is the OFF duty ratio of S_{X1}, r_{LX} is the parasitic resistance of L_X, and r_{X1} and r_{X2} are the on-resistances of S_{X1} and S_{X2},

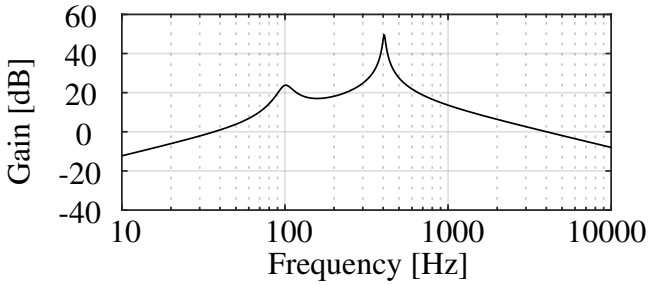


Figure 5.7. Gain-frequency characteristic of $PR(s)\times P(s)$.

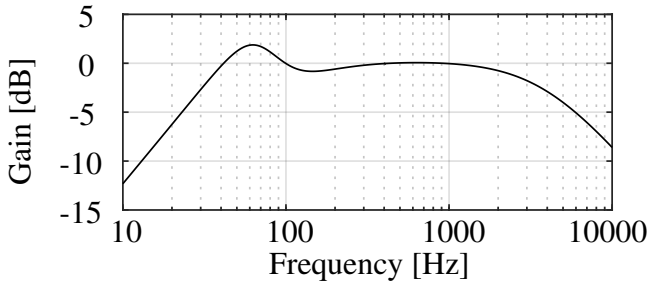


Figure 5.8. Gain-Frequency characteristic of $G_{\mathrm{PX}}(s)$.

respectively.

$$\frac{d}{dt}\begin{bmatrix} \bar{i}_{\mathrm{LX}}(t) \\ \overline{v}_{\mathrm{X}}(t) \\ \overline{v}_{\mathrm{DC}}(t) \end{bmatrix} = A \begin{bmatrix} \bar{i}_{\mathrm{LX}}(t) \\ \overline{v}_{\mathrm{X}}(t) \\ \overline{v}_{\mathrm{DC}}(t) \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ \frac{1}{C_{\mathrm{DC}}} \end{bmatrix} I_{\mathrm{PV}} \tag{5.5}$$

$$A = \begin{bmatrix} -\frac{r_{\mathrm{X}}}{L_{\mathrm{X}}} & \frac{\overline{D}_{\mathrm{X1}}}{L_{\mathrm{X}}} & -\frac{D_{\mathrm{X1}}}{L_{\mathrm{X}}} \\ -\frac{\overline{D}_{\mathrm{X1}}}{C_{\mathrm{X}}} & 0 & 0 \\ \frac{D_{\mathrm{X1}}}{C_{\mathrm{DC}}} & 0 & -\frac{1}{R_{\mathrm{inv}}C_{\mathrm{DC}}} \end{bmatrix} \tag{5.6}$$

$$r_{\mathrm{X}} = r_{\mathrm{LX}} + D_{\mathrm{X1}}r_{\mathrm{X1}} + \overline{D}_{\mathrm{X1}}r_{\mathrm{X2}} \tag{5.7}$$

From (5.5) – (5.7), $P(s)$ can be expressed as shown in (5.8). $P(s)$ has a resonant frequency f_{c} that is determined by L_{X}, C_{X}, and C_{DC}. $P(s)$ has high gain characteristics in the band

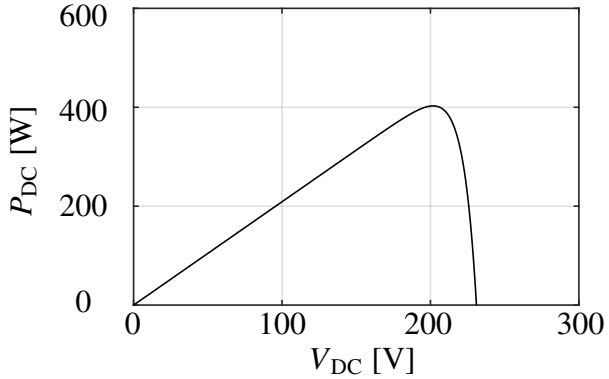


Figure 5.9. PV characteristic for real-time simulation.

around f_c.

$$P(s) = \frac{I_{LX}(s)}{D_{X1}(s)} = \frac{\frac{(V_{DC}+V_X)}{L_X}s}{s^2 + \frac{r_X}{L_X}s + (\frac{D_{X1}^2}{L_X C_{DC}} + \frac{\overline{D}_{X1}^2}{L_X C_X})} = \frac{\frac{(V_{DC}+V_X)}{L_X}s}{s^2 + \frac{r_X}{L_X}s + \omega_c^2} \tag{5.8}$$

Fig. 5.7 shows the gain-frequency characteristics of $PR(s)\times P(s)$. $PR(s)\times P(s)$ has a gain characteristic of more than 10 dB at 100 Hz – 1 kHz based on the resonance and PR compensator characteristics. Fig. 5.8 shows the gain-frequency characteristics of the transfer function $G_{PX}(s)$. The gain characteristics remain near 0 dB in the 100 Hz – 1 kHz band; it was confirmed that the response of the APD control is secured in this band.

5.2 Verification results

It is difficult to verify the control strategies because the power generation characteristics and 3rd harmonic voltage depend on the actual experimental environment. Therefore, the influence of the harmonic voltage on the conventional APD control was verified through real-time simulation. Fig. 5.9 shows the P-V characteristics for real-time simulation.

Fig. 5.10 shows the operating waveform with the conventional APD control of c_f=0.75 and c_h=0. Figs. 5.11 and 5.12 show the operating waveform with the APD control of c_f=1.0, c_h=1.0, and c_f=0.73, c_h=0.51. The waveforms show the inverter output voltage v_{AC}, inverter current i_{AC}, DC voltage v_{DC}, decoupling capacitor voltage v_X, output power

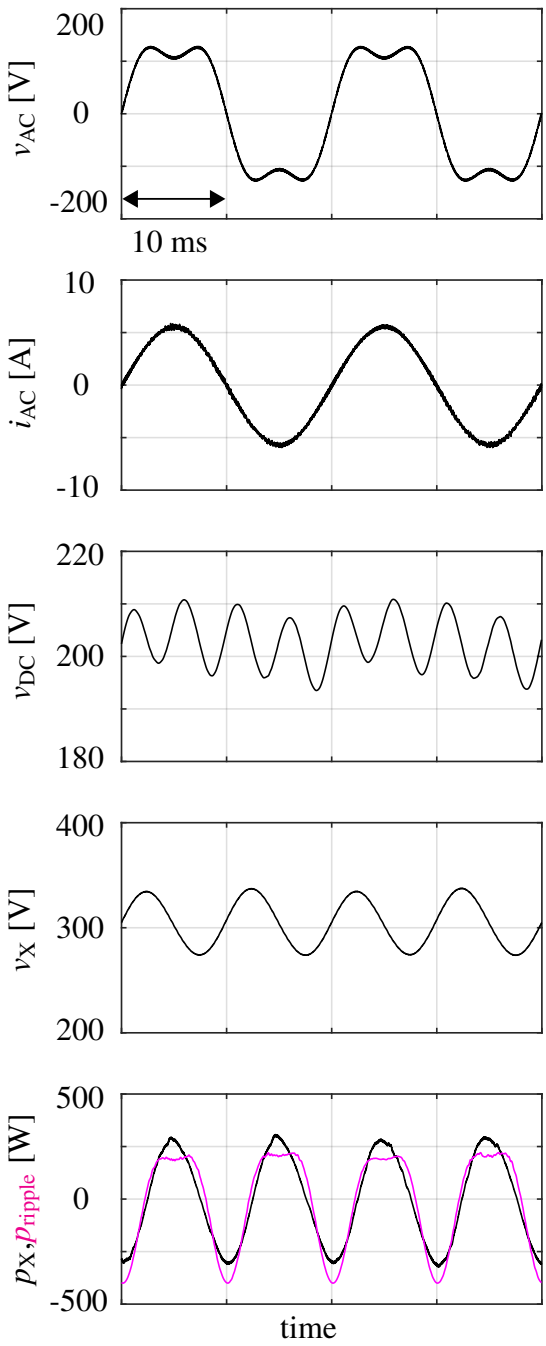


Figure 5.10. Operation waveforms with conventional APD control of c_f=0.75.

pulsation p_{ripple}, and compensating power p_X from the top. A low pass filter is used for v_{DC}, p_X, and p_{ripple} to remove the switching frequency components. The cut-off frequency of low pass filter is designed at 2 kHz.

v_{AC} has harmonic components of the grid voltage. From i_{AC} waveforms, the inverter produces 50 Hz AC current with the conventional and proposed APD control.

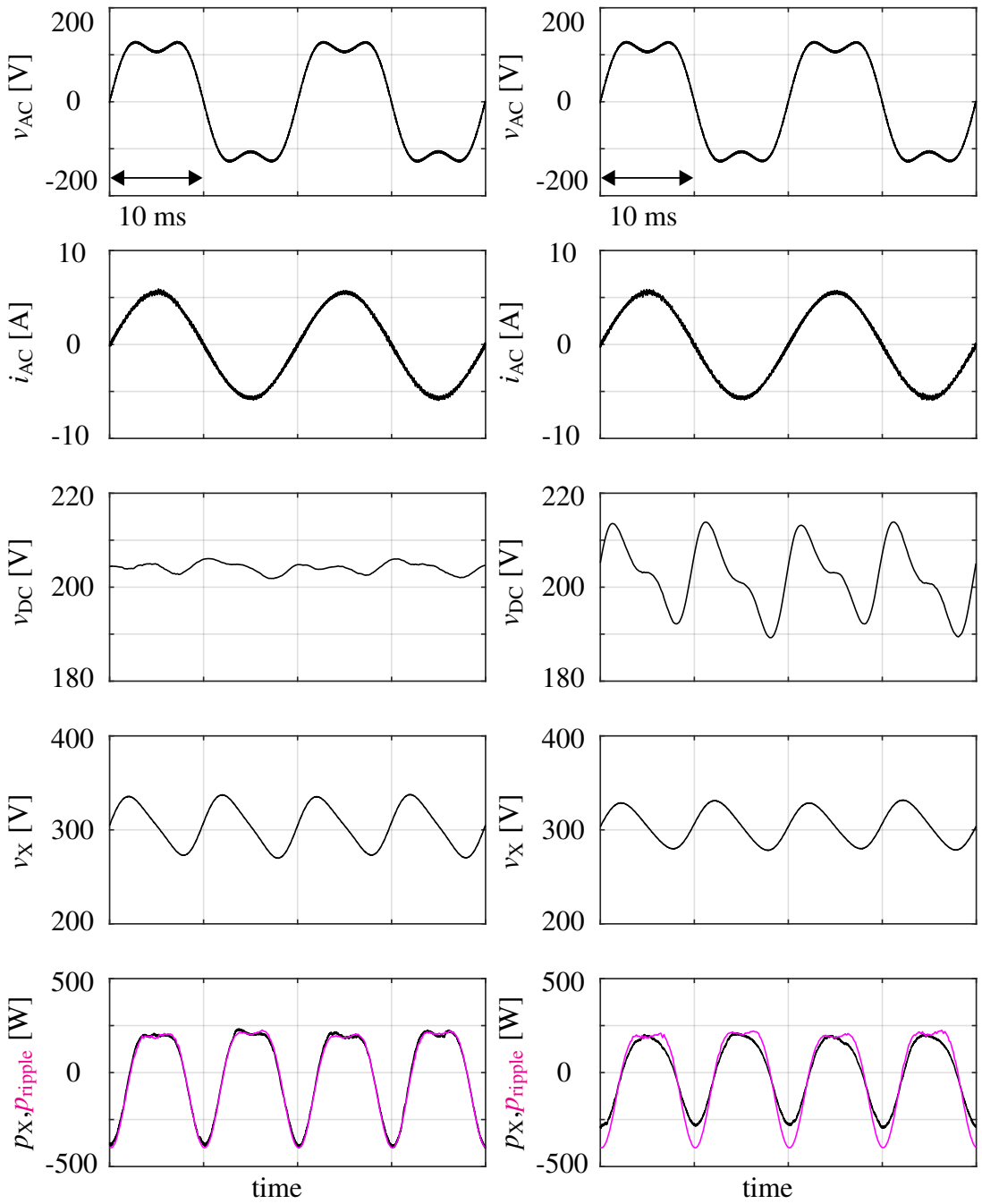


Figure 5.11. Operation waveforms with APD control of c_f=1.0 and c_h=1.0.

Figure 5.12. Operation waveforms with APD control of c_f=0.73 and c_h=0.51.

Fig. 5.13 shows the FFT waveforms of v_{DC} in Fig. 5.10 – 5.12. Table 5.4 lists the verification results of the DC voltage ripple Δv_{DCripn} and voltage volatility α_{VDCrip} calculated from v_{DC}. The conventional APD control suppresses the 100 Hz component but not the 200 Hz component. In the APD control of c_f=1.0 and c_h=1.0, both the 100 and

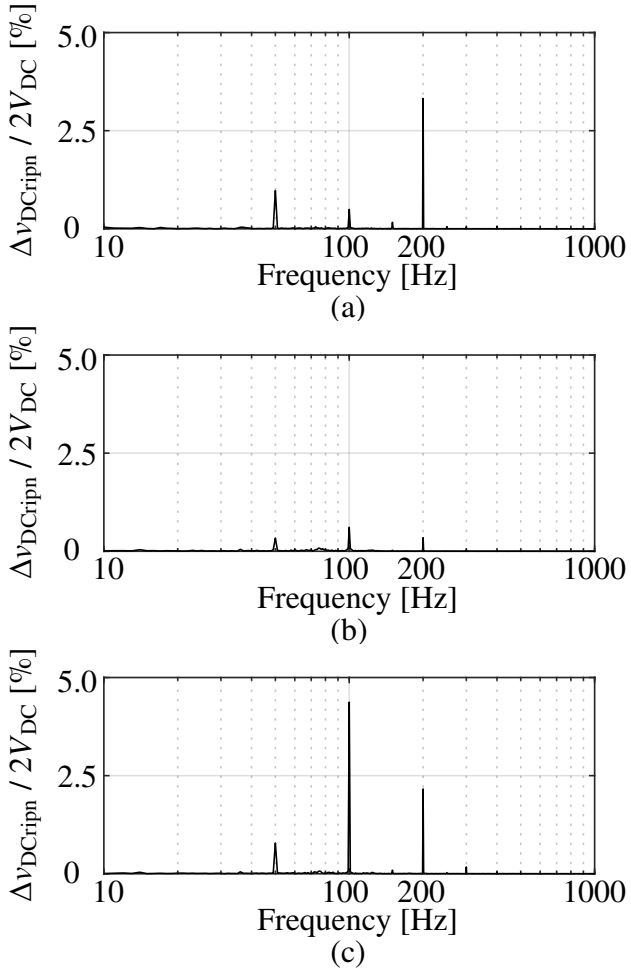


Figure 5.13. FFT waveforms of the DC voltage with the APD control. (a) With the conventional APD control. (b) With the APD control of c_{f}=1.0 and c_{h}=1.0. (c) With the APD control of c_{f}=0.73 and c_{h}=0.51.

200 Hz components are suppressed. In the APD control of c_{f}=0.73 and c_{h}=0.51, α_{VDCrip} is 4.87% because the 100 and 200 Hz components are controlled by the compensation ratios c_{f} and c_{h}.

The pulsation of the 100 Hz component can be confirmed from the v_{X} waveform in Fig. 5.10. The decoupling capacitor voltage v_{X} shows a pulsation of the 200 Hz components as well as the 100 Hz component in Figs. 5.11 and 5.12.

Table 5.5 presents the verification results of the output power pulsation p_{ripple} and compensating power p_{X}. In the conventional APD control, it was confirmed that the 100 Hz component of the output power pulsation is compensated. In the APD control of c_{f}=1.0 and c_{h}=1.0, both the 100 Hz and 200 Hz components are compensated. In the APD

Table 5.4. Verification results of voltage ripple $\Delta v_{\mathrm{DCripn}}$ and voltage volatility α_{VDCrip}.

	$\Delta v_{\mathrm{DCrip2}}$	$\Delta v_{\mathrm{DCrip4}}$	α_{VDCrip}
Conventional APD control of c_{f}=0.75	0.49%	3.32%	3.36%
The APD control of c_{f}=1.0 and c_{h}=1.0	0.61%	0.35%	0.70%
The APD control of c_{f}=0.73 and c_{h}=0.51	4.37%	2.16%	4.87%

Table 5.5. Verification results of output power pulsation p_{ripple} and compensating power p_{X}.

	100 Hz	200 Hz	CP_{ratio}
Output power pulsation p_{ripple}	298.9 VA	97.7 VA	
p_{X} with conventional APD control of c_{f}=0.75	295.4 VA	21.8 VA	94.2%
p_{X} with the APD control of c_{f}=1.0 and c_{h}=1.0	294.1 VA	97.6 VA	98.5%
p_{X} with the APD control of c_{f}=0.73 and c_{h}=0.51	238.6 VA	48.8 VA	77.4%

control of c_{f}=0.73 and c_{h}=0.51, the 100 Hz and 200 Hz components are compensated by the compensation ratios c_{f} and c_{h} to the target values of 79.8% and 49.9%, respectively. Further, it was confirmed that the voltage volatility α_{VDCrip} of 5% could be achieved even when the compensated power was reduced from 98.5% to 77.4%.

5.3 Summary

Chapter 5 described the control strategies of APD for the compensation of power pulsation caused by both fundamental and harmonic components. The verification results confirmed that the APD control compensates for the power pulsation caused by both the fundamental and harmonic components. Additionally, it was confirmed that the compensating power can be reduced from 98.5% to 77.4%. It has an advantage in reducing device loss from suppression of compensating power ratio.

Chapter 6

Real-time Parameter Estimation for Impedance with Resonant Characteristics

This chapter proposes estimation methods of quality factor and LCR parameters for real-time estimation of grid impedance with resonant characteristics to achieve high estimation accuracy. The quality factor estimation method focusing on phase variation near the resonant frequency and the LCR parameter estimation method using quality factor is proposed. In addition, the estimated frequency injection method that estimates only near the resonant frequency in fine frequency increments is proposed to reduce the estimation time. The accuracy of parameter estimation and estimation time is verified using a HILS and microcontroller. From the validation results, the estimation method achieves that the estimation error of LCR parameters is within 2% and the estimation time is 9.42 s. Estimation time is reduced by a factor of 1/5 compared to the conventional method.

6.1 Target System Configuration

6.1.1 Accuracy target value for parameter estimation

This subsection discusses the impact of grid impedance estimation errors on the voltage ripple control proposed in Chapter 3. Chapter 2.4.1 describes the change in voltage ripple

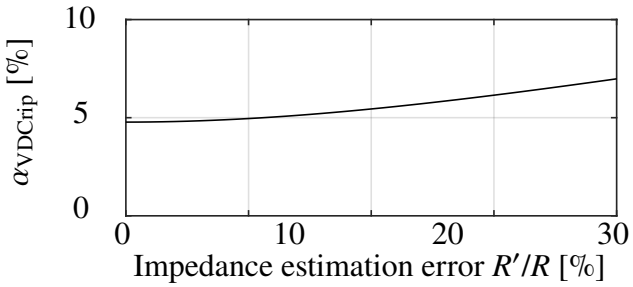


Figure 6.1. Effect of grid impedance estimation error on voltage ripple control with c_f.

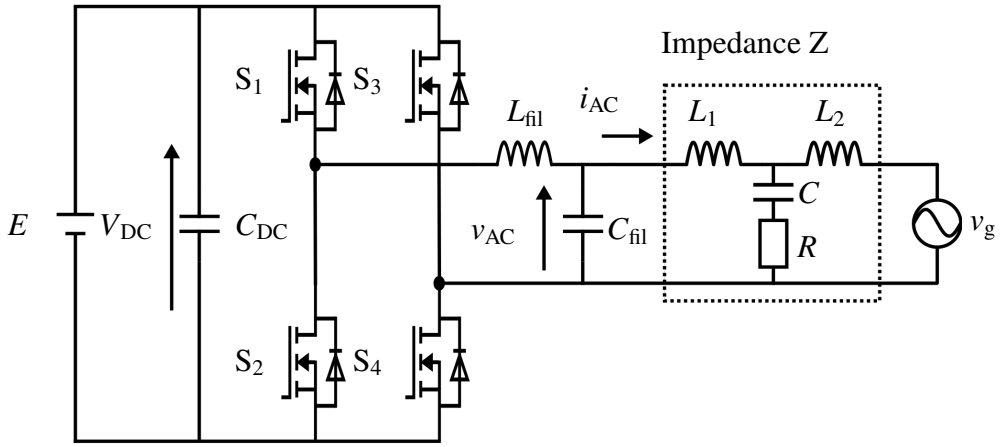


Figure 6.2. Main circuit configuration of impedance estimation.

when grid impedance estimation errors occur, based on (2.13). The compensation ratio c_f in Chapter 3 is introduced in (2.13), which is shown in (6.1).

$$\Delta v_{DCrip} = \frac{I_1 V_1 \{(\cos\theta_p - c_f \cos\theta'_p) + (\sin\theta_p - c_f \sin\theta'_p)\}}{\omega_g V_{DC} C_{DC}} \tag{6.1}$$

Fig. 6.1 shows the effect of impedance estimation error with respect to R on voltage ripple control with c_f at V_1=100 V, I_1=50 A, C_{DC}=50 µF, V_{DC}=200 V, and c_f=0.99. It can be confirmed that the voltage ripple ratio of 5% is maintained when the impedance estimation error is less than 5%. Therefore, an impedance estimation error of 5% or less is required for voltage ripple control.

6.1.2 Target system configuration

Fig. 6.2 shows the main circuit configuration, and Table 6.1 lists the circuit and microcontroller specifications. The main circuit consists of voltage supply E, the grid-connected

Table 6.1. Circuit and microcontroller specifications.

Parameter	Value
Voltage supply E	200 V
Output power P_{AC}	1 kVA
Grid voltage v_{g}	100 V
Grid frequency f_{g}	50 Hz
Switching frequency f_{SW}	20 kHz
Input capacitance C_{DC}	2 mF
Filter inductance L_{f}	2250 µH
Filter capacitance C_{f}	3.3 µF
Grid inductance L_1	400 µH
Grid inductance L_2	300 µH
Load resistance R	150 mΩ
Load capacitance C	300 µF
Bit number of AD converter	16 bit
Flash memory	1024 KB
Voltage detection ratio V_{ratio}	1:200
Voltage range of AD converter V_{range}	6.6 V

inverter, an LC filter, a grid impedance Z, and an AC voltage source v_{g} that simulates the grid. Assuming the case of a power factor correction capacitor connected to the grid, the capacitive component is connected in parallel to the grid. A T-type equivalent circuit is adopted to consider the case where the capacitor is inserted between the grid and inverter. Each LCR parameter is set to a value such that the resonant frequency is between the 2nd and 20th order of the grid frequency, assuming that a large capacitance is installed.

6.2 Parameter Estimation Method

6.2.1 Estimated equation for quality factor

The quality factor is derived from the phase variation near the resonant frequency. Fig. 6.3 shows the equivalent circuit of grid impedance Z. Assuming that the AC voltage source v_{g} is short-circuited, the grid impedance $Z(s)$ is expressed by (6.2).

$$Z(s) = \frac{s^3 L_1 L_2 C + s^2 (L_1 + L_2) CR + s(L_1 + L_2)}{s^2 L_2 C + sCR + 1} \tag{6.2}$$

Fig. 6.4 shows the equivalent circuit considering resonant in the denominator term of

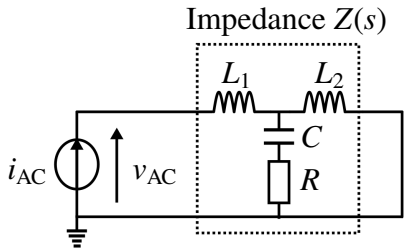


Figure 6.3. Impedance $Z(s)$ equivalent circuit.

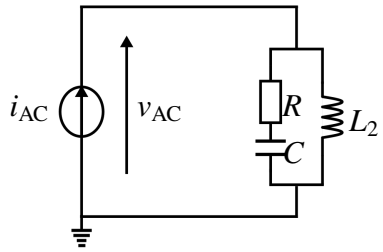


Figure 6.4. Impedance equivalent circuit at resonant angular frequency ω_{r1}.

the impedance model in (6.2). The denominator term is represented by a series resonant circuit of L_2, C, and R. Eq. (6.3) shows the resonant angular frequency ω_{r1}.

$$\omega_{r1} = \frac{1}{\sqrt{L_2 C}} \tag{6.3}$$

The quality factor at resonant frequency Q_{r1} is expressed by (6.4).

$$Q_{r1} = \frac{\omega_{r1}}{\omega_2 - \omega_1} = \frac{1}{R}\sqrt{\frac{L_2}{C}} \tag{6.4}$$

where ω_1 is the angular frequency at which the phase characteristic shifts +45 degree from the phase of the resonant frequency θ_{r1}, and ω_2 is the angular frequency at which the phase characteristic shifts -45 degree from θ_{r1}.

The relationship between phase-frequency characteristics near the resonant frequency and quality factor is clarified. From the equivalent circuit in Fig. 6.4, the impedance characteristics near the resonant frequency $G_{r1}(s)$ can be expressed as in (6.5).

$$G_{r1}(s) = \frac{(s^2 CR + s)/C}{s^2 + sR/L_2 + \omega_{r1}} \tag{6.5}$$

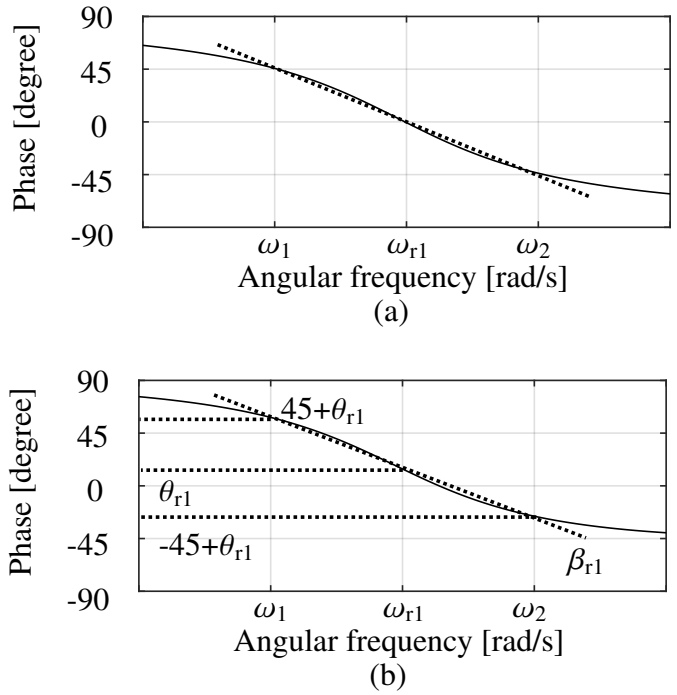


Figure 6.5. Phase-frequency characteristics around ω_{r1} . (a) $G_{r1}(s)$. (b) $Z(s)$.

Fig 6.5(a) shows the phase-frequency characteristic of $G_{r1}(s)$. ω_{r1} has a phase of 0 degree, ω_1 has a phase of 45 degree, and ω_2 has a phase of -45 degree. On the other hand, Fig. 6.5(b) shows the phase-frequency characteristics of $Z(s)$ around the resonant frequency. The phase-frequency characteristic in Fig. 6.5(a) has an offset of θ_{r1}. The phase between ω_1 and ω_2 is assumed to be 90 degrees, and the phase change between ω_1 and ω_2 is assumed to be linear. The phase slope near the resonant frequency β_{r1} can be expressed in terms of the resonant frequency and quality factor Q_{r1} as in (6.6).

$$\beta_{r1} = \frac{2\pi 90}{\omega_2 - \omega_1} = \frac{2\pi 90 Q_{r1}}{\omega_{r1}} \tag{6.6}$$

By obtaining β_{r1} from the phase estimation results near the resonant frequency, the quality factor can be derived from β_{r1} and the resonant angular frequency ω_{r1}.

6.2.2 Estimated equation for LCR parameters

The estimation of the 4 parameters L_1, L_2, C, and R requires 4 equations. These 4 equations are derived by focusing on the characteristics of resonant frequency for the

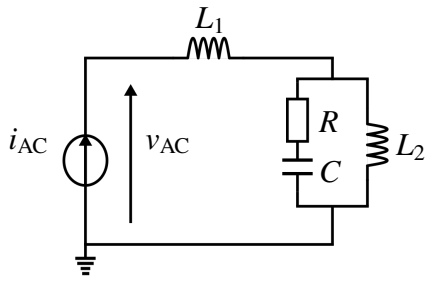


Figure 6.6. Impedance equivalent circuit at resonant angular frequency ω_{r2}.

impedance model in (6.2). Fig. 6.6 shows the equivalent circuit considering resonance in the numerator term of the impedance model in (6.2). The numerator term is represented by a parallel resonant circuit of L_1, L_2, C, and R. Eq. (6.7) shows the resonant angular frequency ω_{r2}.

$$\omega_{r2} = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C}} \tag{6.7}$$

The grid inductance L_{2_r1} is derived from the impedance $|Z_{r1}|$ at the resonant angular frequency, resonant angular frequency ω_{r1} and ω_{r2}, and parameter γ, as shown in (6.8).

$$L_{2\_r1} = \frac{|Z_{r1}|\gamma(\omega_{r2}^2 - \omega_{r1}^2)}{\sqrt{(\omega_{r2}^2 - \omega_{r1}^2)^2 + \omega_{r1}^2 \omega_{r2}^4 \gamma^2}} \tag{6.8}$$

where γ can be expressed from Q_{r1} and ω_{r1}, as shown in (6.9).

$$\gamma = RC = \frac{1}{Q_{r1}\omega_{r1}} \tag{6.9}$$

From equations (6.8) and (6.9), L_{2_r1} can be calculated using ω_{r1}, ω_{r2}, $|Z_{r1}|$ and Q_{r1} detected by impedance estimation.

In addition, L_2 can be expressed in two ways. The grid inductance L_{2_r2} is derived from the impedance $|Z_{r2}|$ at the resonant angular frequency, resonant angular frequencies ω_{r1}

and ω_{r2}, and parameter γ as shown in (6.10)

$$L_{2\_r2} = \frac{|Z_{r2}|(\omega_{r2}^2 - \omega_{r1}^2)}{\gamma\omega_{r2}^4} \times \sqrt{(\omega_{r2}^2/\omega_{r1}^2 - 1)^2 + (\omega_{r2}\gamma)^2} \tag{6.10}$$

From (6.8) and (6.10), the parameter γ exists in the denominator and numerator of both expressions, and an error in γ causes a change in the opposite direction. L_2 can be derived by averaging the two expressions as (6.11), and the estimation error of L_2 can be suppressed.

$$L_2 = (L_{2\_r1} + L_{2\_r2}) * 0.5 \tag{6.11}$$

C and L_1 are derived by using the L_2 as shown in (6.12) and (6.13).

$$C = \frac{1}{L_2\omega_{r1}^2} \tag{6.12}$$

$$L_1 = \frac{L_2\omega_{r1}^2}{\omega_{r2}^2 - \omega_{r1}^2} \tag{6.13}$$

R can be derived from L_2, C, and Q_{r1}, as shown in (6.14).

$$R = \frac{1}{Q_{r1}}\sqrt{\frac{L_2}{C}} \tag{6.14}$$

The parameter estimation is achieved by detecting the five parameters ω_{r1}, ω_{r2}, $|Z_{r1}|$, $|Z_{r2}|$, and Q_{r1} with impedance estimation.

6.3 Impedance estimation method

6.3.1 Estimated frequency injection method

The parameter estimation uses five parameters for resonant frequency: resonant angular frequencies ω_{r1} and ω_{r2}, impedance $|Z_{r1}|$, $|Z_{r2}|$ at the resonant frequency, and Q value Q_{r1}. The detection of resonant frequencies requires estimation in fine frequency increments.

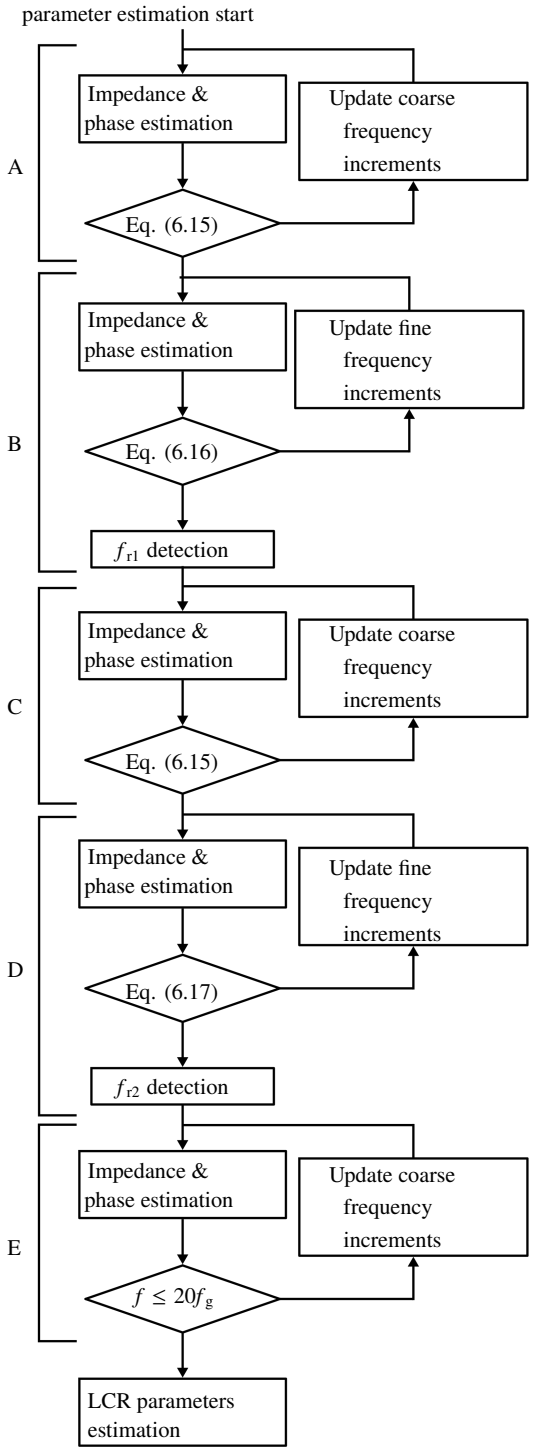


Figure 6.7. Flowchart of parameter estimation.

However, if the estimation is done in fine frequency increments over the range of 100 Hz to 1 kHz, the estimation time increases. Therefore, an estimated frequency injection method is required to perform impedance estimation in fine frequency increments only near the resonant frequency.

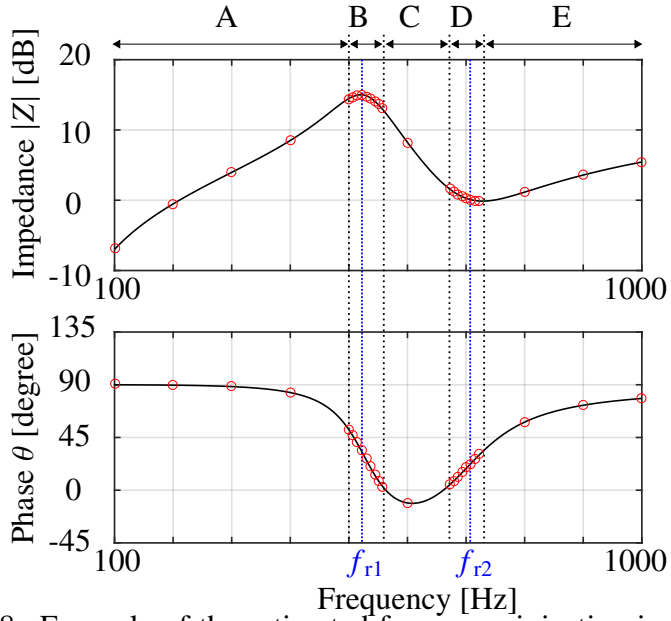


Figure 6.8. Example of the estimated frequency injection in the frequency characteristics of Impedance $|Z|$ and Phase θ.

Fig. 6.7 shows the flowchart of the parameter estimation method. Fig. 6.8 shows the example of the estimated frequency injection in the impedance-frequency characteristics of grid impedance $Z(s)$. In the frequency bands of A, C, and E in Fig. 6.8, estimation is performed in coarse frequency increments to detect the vicinity of the resonant frequency. Determination of the vicinity of the resonant frequency is performed by a positive and negative change in phase θ. Eq. (6.15) represents the phase determination condition.

$$\theta(n-1) \times \theta(n) < 0 \tag{6.15}$$

where n represents the sample point. The frequency between the frequency of phase $\theta(n\text{-}1)$ and the frequency of phase $\theta(n)$ that satisfies (6.15) is determined as the vicinity of the resonant frequency.

In the frequency bands of B and D in Fig. 6.8, estimation is performed in fine frequency increments to detect the resonant frequency. The resonant frequency f_{r1} is detected from the impedance peak, and the resonant frequency f_{r2} is detected from the impedance trough.

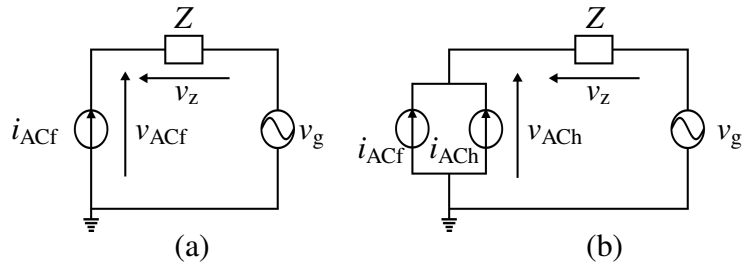


Figure 6.9. Equivalent circuit. (a)Without harmonic current control. (b)With harmonic current control.

Eq. (6.16) represents the impedance peak determination condition.

$$|Z|(n-2) < |Z|(n-1) > |Z|(n) \tag{6.16}$$

The frequency of the impedance peak $|Z|$(n-1) that satisfies (6.16) is detected as f_{r1}. Eq. (6.17) represents the impedance trough determination condition.

$$|Z|(n-2) > |Z|(n-1) < |Z|(n) \tag{6.17}$$

The frequency of the impedance trough $|Z|$(n-1) that satisfies (6.17) is detected as f_{r2}. The impedance estimation with fine frequency increments can be performed only in the necessary frequency bands, thereby reducing the impedance estimation time.

6.3.2 Principle of Impedance Estimation

For impedance estimation, the harmonic amplitude change caused by the harmonic current injection is detected, and the impedance calculation is performed from the amplitude change. The harmonic components in the grid affect the impedance estimation. Refs. [98], [99] proposed suppressing the effects of the grid harmonics by taking differential waveforms before and after harmonic injection. Fig. 6.9 shows the equivalent circuit before and after harmonic injection. Eq. (6.18) expresses the equivalent circuit without harmonics, and (6.19) expresses the equivalent circuit with harmonics.

$$v_{ACf} = Zi_{ACf} + v_g \tag{6.18}$$

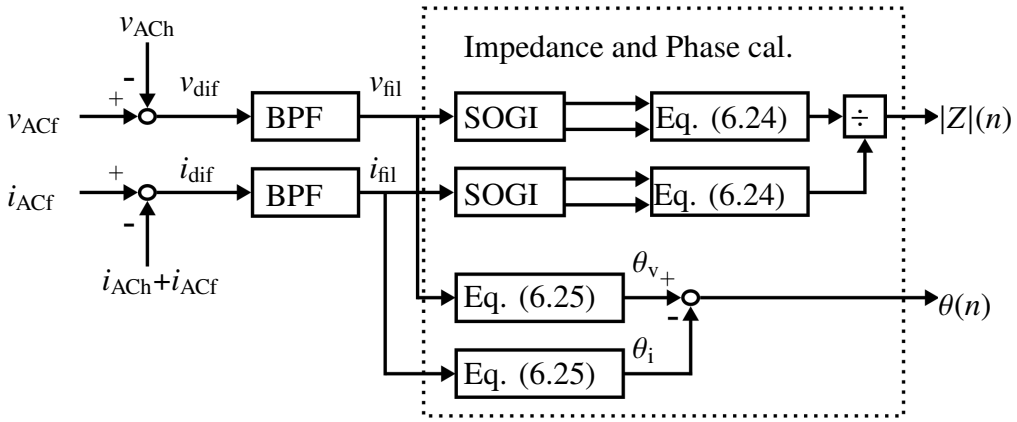


Figure 6.10. Calculation block of impedance and phase.

$$v_{ACf} = Z(i_{ACf} + i_{ACh}) + v_g \tag{6.19}$$

From (6.18) and (6.19), it can be confirmed that the inverter output voltage changes depending on the presence of harmonics. Therefore, the effects of the grid voltage v_g can be suppressed by taking the difference of both voltage and current before and after harmonic injection as in (6.20).

$$\frac{v_{ACh} - v_{ACf}}{(i_{ACh} + i_{ACh}) - i_{ACh}} = \frac{Zi_{ACh}}{i_{ACh}} = Z \tag{6.20}$$

Ref. [99] reported that the difference waveform alone causes variations in the estimated values. It reported that it is necessary to estimate 200 times for one estimated frequency and average the results to achieve an estimation error of about 10 % in impedance estimation using differential waveforms. Grid impedance with resonant characteristics requires the estimation of multiple frequencies to detect characteristics. Therefore, it is required to suppress the variation of the detected waveform in addition to the different waveforms.

6.3.3 Impedance estimation Operation

This thesis proposes impedance estimation with a band-pass filter(BPF) in addition to the difference waveform to suppress the variation of the estimated value. Fig. 6.10 shows a block diagram of the impedance estimation operation. Fig. 6.10 shows a block diagram of

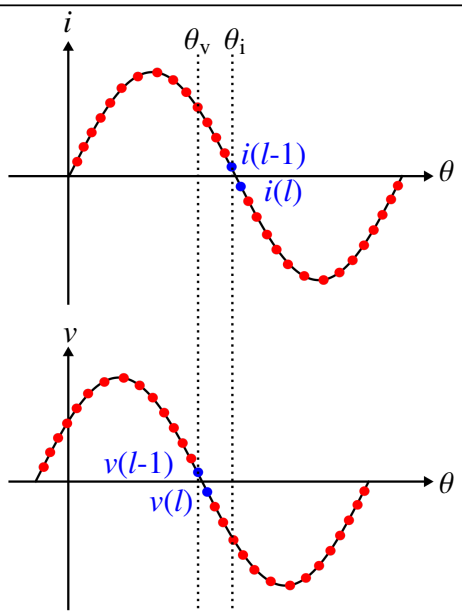


Figure 6.11. Voltage and current sampling.

the impedance estimation operation. In waveform detection, the differential voltage and current waveforms are taken to suppress the influence of the grid, and the amplitude change caused by the inverter control is detected. In addition, a BPF is applied to differential waveforms v_{dif} and i_{dif} to suppress variation in estimated values. Eq. (6.21) shows the BPF.

$$BPF(s) = \frac{2\omega_{\mathrm{b}} s}{s^2 + 2\omega_{\mathrm{b}} s + \omega_{\mathrm{c}}^2} \tag{6.21}$$

where ω_{c} is target angular frequency, and ω_{b} is band angular frequency. The target frequency ω_{c} is varied according to the estimated frequency, and waveform variations can be suppressed regardless of the estimated frequency.

The impedance $|Z|$ is calculated from RMS values of the current I_{rms} and voltage V_{rms}. The filtered waveform v_{fil} and i_{fil} are transformed using a single-phase two-phase transformation. A Second-Order Generalized Integrator(SOGI) is used for the single-phase to two-phase transformation [105]. SOGI is a single-phase to two-phase conversion technique that uses (6.22) and (6.23) to convert a single-phase waveform v_{fil} into a two-

Table 6.2. Breakdown of estimation time.

	Coarse estimation	Fine estimation
Detection of steady-state waveform	1 period	1 period
Convergence of filter cal.	4 periods	4 periods
Impedance & Phase cal.	1 period	10 periods
Total	6 periods (0.12 s)	15 periods (0.3 s)

phase orthogonal waveform v_α and v_β.

$$v_\alpha = \frac{k\omega s}{s^2 + k\omega s + \omega^2} v_{\text{fil}} \tag{6.22}$$

$$v_\beta = \frac{k\omega}{s^2 + k\omega s + \omega^2} v_{\text{fil}} \tag{6.23}$$

I_{rms} and V_{rms} are calculated from the two-phase waveform as shown in (6.24).

$$V_{\text{rms}} = \sqrt{v_\alpha^2 + v_\beta^2} \tag{6.24}$$

|Z| is calculated by dividing V_{rms} by I_{rms} as shown in Fig. 6.10.

The impedance phase θ is derived from the difference of the zero crossing points of the filter waveform. Fig. 6.11 shows an example of voltage and current sampling. The sampling point that satisfies the conditional expressions in (6.25) is defined as the zero-crossing point of the voltage and current waveforms.

$$v(l) < v(l-1) \& v(l) \times v(l-1) < 0 \tag{6.25}$$

θ is calculated from the difference between voltage phase θ_{v} and current phase θ_{i} as shown in Fig. 6.10. The phase slope β_{rl} is derived by applying the least-squares method in a first-order equation and using the phase between the frequency detected as the resonant point and the frequency four samples before that frequency.

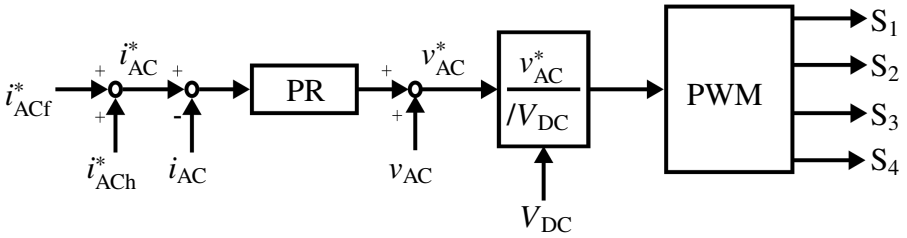


Figure 6.12. Block diagram of fundamental and harmonic current control.

Table 6.2 shows the breakdown of the estimation time. The steady-state waveforms i_{ACf} and v_{ACf} are detected for one period and stored in the array data. A harmonic current is injected, and the difference and filter waveforms are calculated. The impedance and phase need to be calculated after the BPF calculation has converged. The filter calculation convergence time is set to 4 periods based on 100 Hz, which takes the longest time for the BPF calculation to converge. After the filter calculation converges, the impedance and phase are calculated. Repeated impedance estimation is performed and averaged to suppress variation in the estimated values. In coarse frequency increments, number of repetitive periods is set to 1 because the purpose is to detect the vicinity of the resonant frequency, and high estimation accuracy is not required. In fine estimated frequency increments, number of repetitive periods is set to 10 because high estimation accuracy is required to detect the impedance, phase, and frequency of the resonant point.

6.3.4 Harmonic current injection method

The single injecting frequency is employed as the injection harmonic current of uniform amplitude regardless of the estimated frequency. Fig. 6.12 shows a block diagram of the fundamental and harmonic current control. The configuration of the PR compensator is shown in (6.26), which has a term for the harmonic component to be controlled in addition to the term for the fundamental component.

$$PR(s) = K_P + \frac{K_{Rf} 2\omega_{bf} s}{s^2 + 2\omega_{bf} s + \omega_f^2} + \frac{K_{Rh} 2\omega_{bh} s}{s^2 + 2\omega_{bh} s + \omega_h^2} \tag{6.26}$$

Table 6.3. Frequency increments of impedance estimation.

Coarse frequency increments	100 Hz
Fine frequency increments	5 Hz

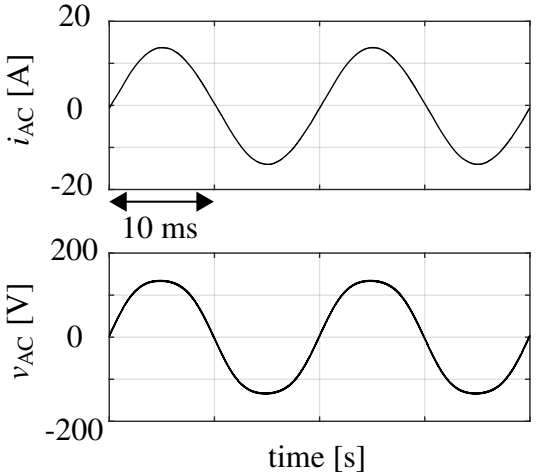


Figure 6.13. Operating waveform without harmonic current control.

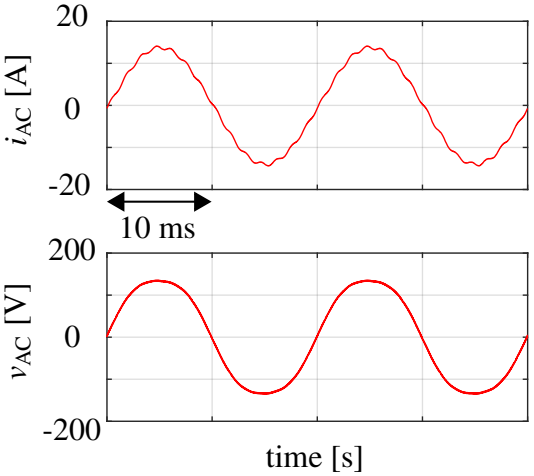


Figure 6.14. Operating waveform with harmonic current control.

where K_P is proportional gain, K_{Rf} is resonant gain of fundamental frequency, K_{Rh} is resonant gain of harmonic frequency, ω_f is fundamental angular frequency, ω_h is harmonic angular frequency, ω_{bf} is fundamental band angular frequency, ω_{bh} is harmonic band angular frequency. The addition of the harmonic component term provides a harmonic current output with uniform amplitude regardless of the estimated frequency. The harmonic component term is updated at the time when the estimation frequency is switched. Harmonic current with 3 % of the fundamental current RMS value is injected into Z.

6.4 Verification result

The impedance estimation system using a microcontroller and a real-time simulator was constructed, and the estimation of grid impedance with resonant characteristics was verified by the impedance estimation system. Table 6.3 lists each frequency increments of impedance estimation. A coarse frequency increments is performed at 100 Hz, and a fine frequency increments is performed at 5 Hz. The operation of the harmonic current control by the inverter is confirmed from the operation waveform at 700 Hz control as a value near f_{r2}. Figs. 6.13 and 6.14 show the inverter output current i_{AC} and voltage

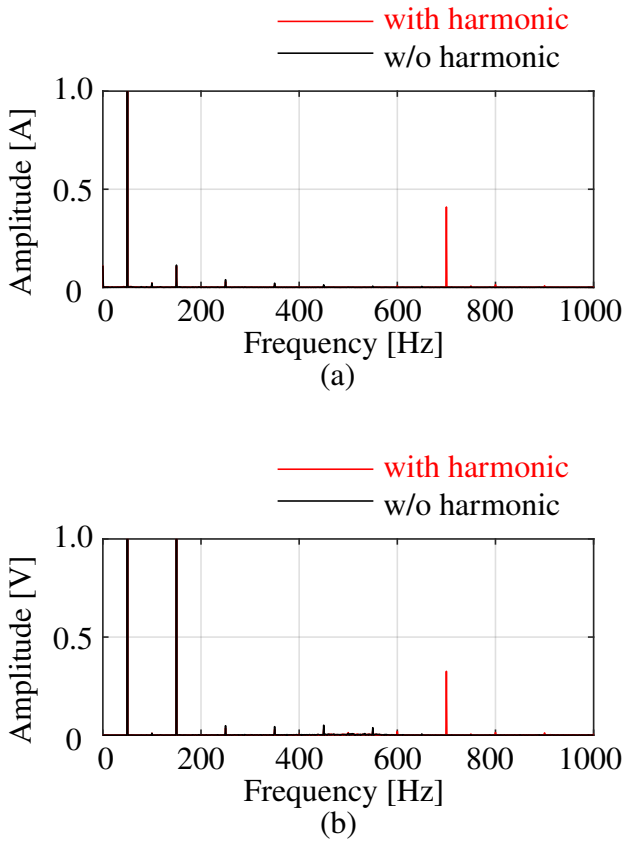


Figure 6.15. FFT waveform. (a) Output current i_{AC}. (b) Output voltage v_{AC}.

v_{AC} waveforms with and without harmonic current control. The injection of harmonic components can be confirmed. Fig. 6.15 shows the FFT waveforms of the inverter output current and voltage. Fig. 6.15 (a) shows that the 700 Hz component has an amplitude of about 0.41 A (2.96 %) owing to the harmonic current control. Fig. 6.15 (b) also shows the amplitude change in the 700 Hz owing to the harmonic current control. The voltage resolution of AD converter V_{res} is defined by (6.27), where V_{range} is the voltage range of AD converter, and V_{ratio} is the voltage detection ratio.

$$V_{\mathrm{res}} = \frac{V_{\mathrm{ratio}} \times V_{\mathrm{range}}}{2^{16}} \tag{6.27}$$

The resolution of the AD converter V_{res} is calculated to be 0.02 V from the conditions in Table 6.1. The voltage amplitude of 0.33 V at 700 Hz indicates that sufficient harmonic

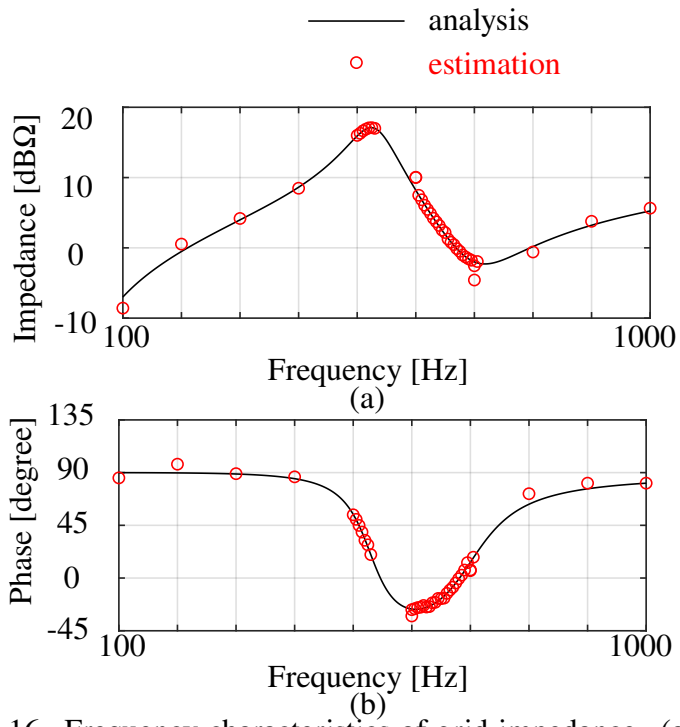


Figure 6.16. Frequency characteristics of grid impedance. (a) Impedance-Frequency characteristics. (b) Phase-Frequency characteristics.

Table 6.4. Number of impedance estimation points and estimation time.

Number of estimated points at coarse frequency increments (0.12 s)	11 (1.32 s)
Number of estimated points at fine frequency increments (0.3 s)	27 (8.1 s)
Estimation time	9.42 s

current is injected into the grid impedance.

Fig. 6.16 shows a comparison between the impedance estimation results and the numerical analysis values. The numerical analysis value is calculated in (6.2). From Fig. 6.16 , it can be confirmed that the impedance-frequency characteristics can be obtained near the resonant frequency. Table 6.4 shows the number of impedance estimation points and estimation time. In the impedance estimation, 38 points are estimated, and the frequency characteristics are obtained in 9.42 s.

Validation of parameter estimation using estimation results of impedance-frequency characteristics is also performed. The parameter estimations are performed 200 times, and

Table 6.5. Estimation result of parameters for the calculation using phase θ_{r1}.

Analytical value	Average value	Average value error	Standard deviation
$\|Z_{r1}\|$= 7.06 Ω	7.16 Ω	1.4%	0.02 Ω
$\|Z_{r2}\|$= 0.79 Ω	0.76 Ω	-3.8%	0.06 Ω
f_{r1} = 530.5 Hz	525.0 Hz	-1.04%	0 Hz
f_{r2} = 701.8 Hz	697.1 Hz	-0.7%	6.59 Hz
θ_{r1} = 19.3 degree	26.5 degree	37.3%	0.6

Table 6.6. Estimation result of LCR parameters by using phase θ_{r1}.

True value	Average value	Average value error	Standard deviation
R= 150.0 mΩ	225.8 mΩ	50.5%	11.5 mΩ
L_1 = 400.0 µH	416.0 µH	4.0%	17.1 µH
L_2 = 300.0 µH	317.1 µH	5.7%	6.3 µH
C= 300.0 µF	289.9 µF	-3.4%	5.7 µF

the average value, error of the average value, and the standard deviation are derived. Eq. (6.28) shows the average value of the estimated value $L_{average}$, (6.29) shows the estimation error of the average estimated value L_{error}, and (6.30) shows the standard deviation of the estimated value L_{sd}. Where n is the number of parameter samplings.

$$L_{average} = \frac{1}{n}\sum_{k=1}^{n} L_{estimation}(k) \tag{6.28}$$

$$L_{error} = \frac{L_{average}}{L_{true\_value}} * 100 \tag{6.29}$$

$$L_{sd} = \sqrt{\frac{1}{n}\sum_{k=1}^{n}(L_{estimation}(k) - L_{average})^2} \tag{6.30}$$

Table 6.5 shows the estimation results of parameters for the calculation, and Table 6.6

Table 6.7. Estimation result of parameters for the calculation using quality factor Q_{r1}.

Analytical value	Average value	Average value error	Standard deviation
$\|Z_{r1}\|$= 7.06 Ω	7.16 Ω	1.4%	0.01 Ω
$\|Z_{r2}\|$= 0.79 Ω	0.75 Ω	-5.1%	0.05 Ω
f_{r1} = 530.5 Hz	525.0 Hz	-1.04%	0 Hz
f_{r2} = 701.8 Hz	698.7 Hz	-0.13%	5.0 Hz
β_{r1} = 1.13	1.16	2.7%	0.03
Q_{r1}= 6.67	6.76	1.3%	0.19

Table 6.8. Estimation result of LCR parameters by using quality factor Q_{r1}.

True value	Average value	Average value error	Standard deviation
R= 150.0 mΩ	147.8 mΩ	-1.5%	5.3 mΩ
L_1 = 400.0 µH	393.1 µH	-1.7%	16.0 µH
L_2 = 300.0 µH	302.8 µH	0.9%	7.5 µH
C= 300.0 µF	303.5 µF	1.1%	7.6 µF

shows the parameter estimation results. Table 6.5 shows that each parameter is detected within an error of 37.3%. The frequency detected as the resonant point is different from the resonant frequency of the analysis value, thus an error of more than 30 % is observed in the phase estimation value. The standard deviation confirms that the variability of the estimated values is within 7.6% of the average value. Table 6.6 shows that L_1, L_2, C, and R can be estimated within 50.5% error. The phase estimation error causes an error of more than 50% in the estimated value of R.The standard deviation confirms that the variability of the estimated values is within 5.1% of the average value.

Table 6.7 shows the estimation results of parameters for the calculation, and Table 6.8 shows the parameter estimation results. Table 6.7 shows that each parameter is detected within an error of 5.1%, although each resonant frequency is detected at a value different from the analytical value. The standard deviation confirms that the variability of the

estimated values is within 6.7% of the average value. Table 6.8 shows that L_1, L_2, C and R can be estimated within 1.7% error. The standard deviation confirms that the variability of the estimated values is within 4.1% of the average value.

6.5 Summary

Chapter 6 described the estimated frequency injection method for real-time parameter estimation of grid impedance with resonant characteristics. The impedance estimation was verified under the estimation conditions of a 16-bit AD converter and a sampling frequency of 40 kHz. It was confirmed that the estimation accuracy of LCR parameters was within 2%, and the estimation time was 9.42s. The 2% estimation error indicates that the effect on voltage ripple control can be sufficiently suppressed.

Chapter 7

Summary and Future Works

7.1 Summary

This dissertation proposed active power decoupling method focusing on PV generation characteristics and distributed power gird. The challenges addressed in each chapter are described below.

Chapter 2 describes related research and clarifies issues that require solutions. Many studies on improving the efficiency of APD method have focused on the circuit scheme. On the other hand, there have been few studies on operation methods such as controlling the compensating power of the APD circuit based on the operating power and power generation characteristics of the PV array. This dissertation proposes a control scheme to control the compensating power of the APD circuit according to the power generation characteristics of the PV array to achieve higher efficiency of the PV system. The importance of considering an integrated system of the partial shade compensation and APD method was demonstrated by describing GCC. The impact of grid harmonic voltage on APD control was clarified, and the study of including power pulsation caused by grid harmonic voltage in compensated power control was shown to be necessary. Furthermore, the influence of grid impedance on APD control was clarified, and the technique for obtaining grid impedance in real time was shown to be necessary. The literature on conventional grid impedance was reviewed, and it is necessary to develop a parameter estimation technique for grid impedance with resonant characteristics.

Chapter 3 describes the compensating power control for APD control focusing on PV power generation characteristics. In a 1 kW rated inverter, the difference and usefulness of the pulsation compensation of the proposed APD control were verified for two capacitance design methods: When C_{DC}=50 µF, the compensation power of 100% by the APD control is required at rated power, but this is much lower than that of 300 µF. The APD control is effective in downsizing the inverter because it uses a small capacitor. On the other hand, when C_{DC}=300 µF, although the capacitance increases, the maximum current capacity is suppressed to 80% of 1 kW operation, enabling the use of switching devices with lower current capacity than in the conventional APD control. In addition, the system efficiency is improved by 1.2–16.8% at operating power of 400 W or less. This is significant in seasons and regions with low solar radiation and long hours of light-load operation. These results show the difference in the amount of compensating power and the usefulness of the proposed APD control depending on the design method of the DC capacitance.

Chapter 4 described two configurations of PV inverters with GCC and APD features. Mathematical analysis was performed on both circuits using the state-space averaged method to clarify the dynamic characteristics of the APD control of both circuits. Furthermore, the disturbance suppression characteristics of the APD control were evaluated using dynamic characteristic analysis, and the differences in control characteristics depending on the configurations were outlined. The operation of the GCC suppressed partial shade and improved the power generation efficiency from 78.6% to 99.5%. In addition, the individual circuit was confirmed to be a more suitable circuit configuration for the PV system in view of its power generation efficiency.

Chapter 5 described the control strategies of APD for the compensation of power pulsation caused by both fundamental and harmonic components. The verification results confirmed that the APD control compensates for the power pulsation caused by both the fundamental and harmonic components. Additionally, it was confirmed that the compensating power can be reduced from 98.5% to 77.4%. It has an advantage in reducing device loss by suppressing the compensating power ratio.

Table 7.1. Summary of the dissertation

	PPD method	Conventional APD method	Proposed APD method
PV generation efficiency (with partial shade)	78.6%	78.6%	99.5% (Chapter4)
System efficiency	76.4%	74.6%	95.4% (Chapter3)
Lifetime of capacitor	110,000 hour (13 years)	200,000 hour (23 years)	200,000 hour (23 years)
Harmonic voltage	No effect	No compensation	Suppression of device loss (Chapter5)
Resonant Impedance	No effect	No compensation	Suppression of influence on voltage ripple control (Chapter6)

Chapter 6 described the estimated frequency injection method for real-time parameter estimation of grid impedance with resonant characteristics. The impedance estimation was verified under the estimation conditions of a 16-bit AD converter and a sampling frequency of 40 kHz. It was confirmed that the estimation accuracy of LCR parameters was within 2%, and the estimation time was 9.42s. From verification results, the estimation method achieves the high estimation accuracy of LCR parameters. The 2% estimation error indicates that the effect on voltage ripple control can be sufficiently suppressed.

Table 7.1 provides a summary of the results of each chapter. It is confirmed that the proposed APD method has high system efficiency compared to the PPD and conventional APD methods.

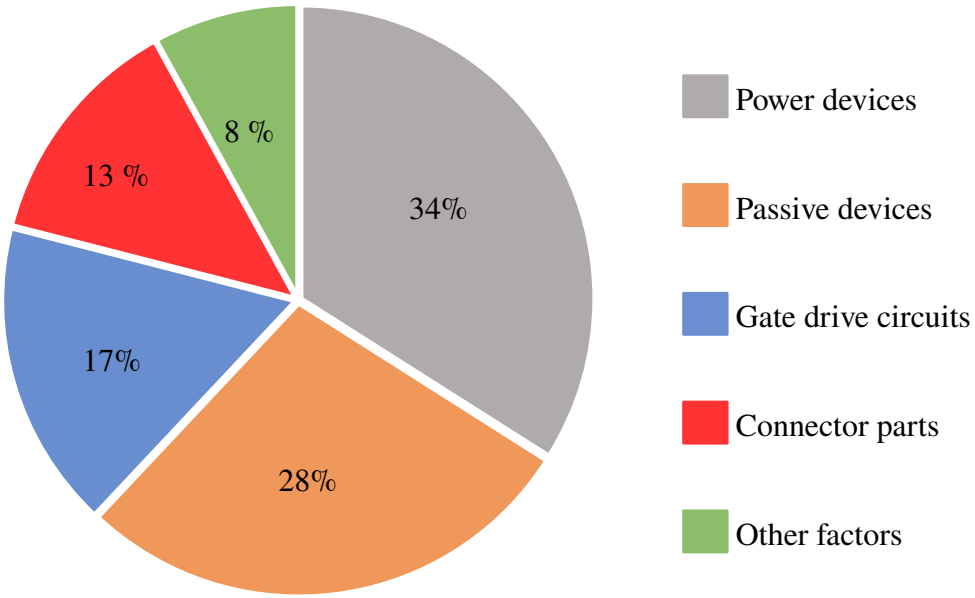


Figure 7.1. Inverter Failure Factors

7.2 Future works

7.2.1 Lifetime evaluation of PV systems with APD method including power devices

Conventional PV systems with APD feature focus on the lifetime of the capacitor. Fig. 7.1 shows the breakdown of inverter failure factors [106]. Power devices account for a large proportion of the failure factors in inverters. Therefore, it is necessary to consider the lifetime of not only the capacitors but also the power devices. Previous studies on inverters have reported that the lifetime of inverters can be improved by operating them with reduced operating power [107].

Therefore, quantitative evaluation of the effect of the suppression of the compensated power ratio by the APD control proposed in this dissertation on the lifetime of the power devices will clarify the lifetime of the entire PV system with APD feature. By comparing with the conventional APD system, it is clarified that the proposed APD system works effectively on the lifetime of the power device.

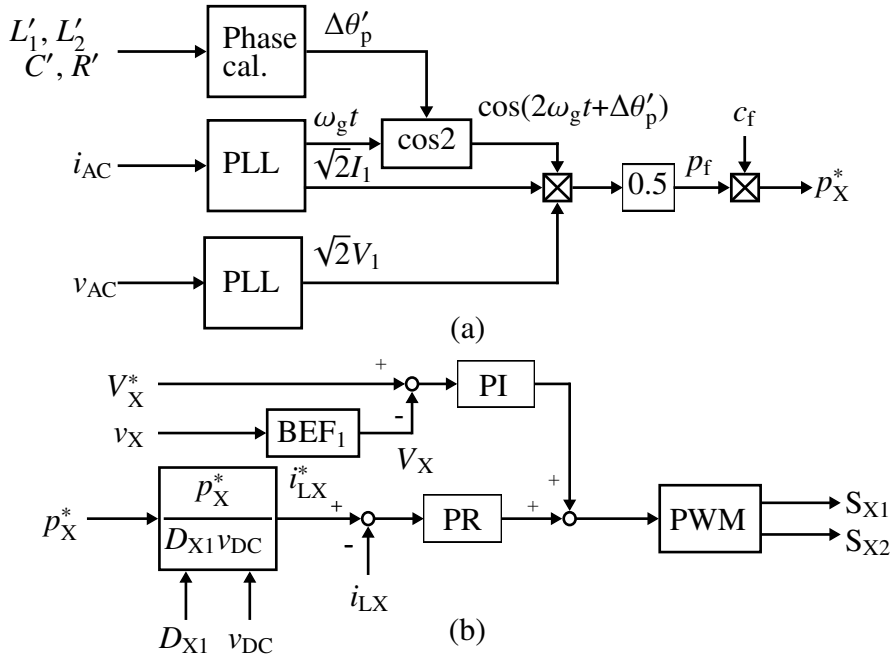


Figure 7.2. Block diagram of the APD control with impedance estimation. (a) Compensating power calculation block. (b) Control block of inductor current i_{LX} and average decoupling capacitor voltage V_X.

7.2.2 Development of design approaches for APD circuits, including DC capacitance

In Chapter 3, the DC capacitance was designed to achieve a voltage ripple ratio of 5% for the operating power, even when the APD circuit is stopped, and the improvement in system efficiency was verified. The design of DC capacitance should also incorporate the concept of volume, since the installation area in a house is limited and power conversion circuits are required to be smaller in volume. In addition, in the proposed method, DC capacitance affects the design of cooling components because of the suppression of device losses associated with the suppression of the compensation power ratio according to DC capacitance. Therefore, the development of a design method for DC capacitance that simultaneously considers system efficiency and the volume of the power conversion circuit is developed.

7.2.3 Verification of the actual system integrating the APD circuit

and GCC

Future studies include verification of the actual system integrating the APD circuit and GCC. The integrated and the individual circuits each have different elements such as power devices and inductor designs. Actual equipment verification including these elements will be performed to verify the circuit characteristics including power conversion efficiency.

7.2.4 Integration of impedance estimation methods and APD control

In Chapter 6, the LCR parameter estimation of the grid impedance with resonant characteristics was verified and a parameter estimation error of 2% was achieved. The application to APD control is shown in Fig 7.2. The phase $\Delta\theta'_{\mathrm{p}}$ is calculated based on the estimated parameters L'_1, L'_2, C', and R' and used for phase compensation of the compensated power command p^*_{X}. It is necessary to verify the operation of the PV system with APD feature when this control system combining impedance estimation and APD control is used. The usefulness of the proposed system will be clarified by discussing the tracking performance of the proposed system with respect to the time variation of the grid impedance.

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