TOKYO METROPOLITAN UNIVERSITY

DOCTORAL DISSERTATION

Laminated Busbar Design for High-Speed Switching of Power Conversion Circuits

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A thesis submitted in partial fulfillment of the requirements
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in the

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Department of Electrical Engineering and Computer Science

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Declaration of Authorship

I, Koji MITSUI, declare that this thesis titled, "Laminated Busbar Design for High-Speed Switching of Power Conversion Circuits" and the work presented in it are my own. I confirm that:

- This work was done wholly or mainly while in candidature for a research degree at this University.
- Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated.
- Where I have consulted the published work of others, this is always clearly attributed.
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TOKYO METROPOLITAN UNIVERSITY

Abstract

Department of Electrical Engineering and Computer Science

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Doctor of Philosophy

Laminated Busbar Design for High-Speed Switching of Power Conversion Circuits

by Koji MITSUI

According to the "Green Growth Strategy for Carbon Neutrality in 2050," research on next-generation power semiconductors (GaN, SiC, etc.) is based on the scenario of expanding their introduction and entering the independent commercial phase after 2025, with power conversion circuit technology playing a role. For example, the use of next-generation power semiconductors in power conversion circuits for electric aircraft and vehicles is accelerating, aiming for further miniaturization and lower loss. Fast switching, a feature of next-generation power semiconductors, has been the subject of many research reports as a technology for reducing power loss in power conversion circuits; however, problems related to fast switching have also emerged. Many of these problems are caused by parasitic inductance in the wiring. Parasitic inductance generates an induced electromotive force (EMF) for the current change (di/dt) of a power device switching at high speed. This induced EMF can be applied to the power device beyond the rated voltage, which has been considered a problem by many research reports. One way to address this problem is to reduce the parasitic inductance of the wiring. Parasitic inductance in wiring exists in the internal wiring and terminals of devices such as power devices and capacitors; hence, there has been a lot of research on reducing this inductance. Furthermore, parasitic inductance also exists in the wiring called busbars that electrically connect these devices. Therefore, it is necessary to reduce the parasitic inductance of busbars to fully utilize the performance of next-generation power semiconductors. To reduce the parasitic inductance of busbars, laminated busbars, which consist of flat conductors sandwiched between insulating materials, are used. Most of the research on laminated busbars has focused on simple structures, but some studies have reported that the connection holes and the distance between terminals required for connecting elements have a significant impact on the parasitic inductance. While laminated busbars can reduce parasitic inductance, their structure increases parasitic capacitance. This parasitic capacitance, together with the parasitic inductance, forms a resonant circuit that causes large voltage and current oscillations during switching. Furthermore, because of these parasitic parameters, when multiple capacitors are connected, the current flowing through each capacitor is reported to be unbalanced. Thus, many studies on laminated busbars and the reduction of parasitic inductance have been reported, but it is impossible to reduce the parasitic parameters to zero

owing to the physical constraints of the structure. In other words, the design of power conversion circuits must allow for a certain amount of parasitic parameters. In conventional silicon semiconductors, the effect of parasitic inductance was within the acceptable range; however, in next-generation power semiconductors, it is necessary not only to reduce parasitic inductance but also to design appropriately. However, laminated busbars are focused only on reducing parasitic inductance, and no clear design guidelines for parasitic parameters have yet been provided. In addition, detailed structures such as terminal hole diameter and distance between terminals are currently designed based on the circuit designer's rule of thumb, which makes them unsuitable for higher switching speeds.

The objective of this study is to establish a laminated busbar design method to realize high-speed switching. This study proposes a design method to solve the problems caused by fast switching and parasitic parameters, and clarifies the effectiveness of the proposed method through experiments. This thesis is divided into six chapters, each of which is summarized below.

Chapter 1 describes the necessity of this study in terms of social and technological backgrounds. It also clearly states the issues and objectives of this study.

In Chapter 2, the related and previous studies of this research are summarized to clarify the high-speed switching issues to be addressed in this research. Unlike the previous studies in which parasitic inductance and capacitance are considered, this study considers parasitic resistance and parasitic conductance as well as their effects are discussed. A literature survey reveals that the parasitic parameters and fast switching challenges are surge voltage, oscillation, and unbalance.

Chapter 3 analyzes the current unbalance that occurs in capacitors connected in parallel to laminated bus bars. The parasitic parameter of the hole diameter at the busbar terminal, which is one of the causes of current unbalance, is calculated by electromagnetic field analysis, and its effect on current unbalance is summarized. Based on the results, we solved the problem of unbalance by presenting a design method for appropriate hole diameters for the operating conditions.

Chapter 4 describes the vibration phenomenon after switching from the viewpoint of laminated busbar design. Vibration phenomena occur mainly from a few MHz to about 100 MHz, and it is clear that factors such as skin effect and proximity

effect are significant. Therefore, an equivalent circuit including parasitic resistance and parasitic conductance is applied. Using the equivalent circuit, a design method for a laminated busbar structure that suppresses vibration phenomena within a target value in terms of time and frequency axes is presented to solve the vibration problem.

Chapter 5 describes a design method for laminated busbar structures that can be designed simultaneously with conventional surge voltage, in addition to the vibration phenomena described in Chapter 4. It is clarified that parasitic inductance affects surge voltage and parasitic capacitance affects oscillation phenomena and that these are trade-offs. A design method is then proposed to integrate these different dimensions into a single design method. Experimental verification using a 400 V, 30 A buck chopper circuit is conducted to demonstrate the effectiveness of the proposed method. The method simultaneously solves the vibration and surge voltage issues in the design of laminated busbar structures.

Chapter 6 presents the conclusions of this thesis from the results obtained in the previous chapters. The impact of this research on the power conversion field as well as the future prospects are also discussed.

Acknowledgements

I would like to express my deep and sincere gratitude to my research supervisor, Professor Keiji Wada for giving me the opportunity to do research and providing invaluable guidance throughout this research. His dynamism, vision, sincerity and motivation have deeply inspired me. I would also like to thank him for his friendship, empathy, and great sense of humor.

I am extremely grateful to the Ph.D. defense committee members, Professor Takanori Isobe, Shigeyoshi Goka, and Yukihisa Suzuki for taking out valuable time for my defense. I appreciate their insightful and critical comments.

I thank my friends and research colleagues for their constant encouragement. They have been a great source of comfort, love, and inspiration since I met them.

Lastly, I would be remiss in not mentioning my family for supporting me anytime. Their belief in me has kept my spirits and motivation high during this process.

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List of Abbreviations

AEA	**A**ll **E**lectric **A**ircraft
BEV	**B**attery **E**lectric **V**ehicle
DFT	**D**iscrete **F**ourier **T**ransform
EECS	**E**lectrical **E**nvironmental **C**ontrol **S**ystem
EM	**E**lectro **M**agnetic
EMAs	**E**lectro**M**echanical **A**ctuators
EV	**E**lectric **V**ehicle
FEM	**F**inite **E**lement **M**ethod
FP	**F**uel **P**umps
GaN	**Ga**llium **N**itride
GHG	**G**reen **H**ouse **G**as
HEV	**H**ighbrid **E**lectric **V**ehicle
HPD	**H**igh **P**ower **D**ensity
ICE	**I**nternal **C**ombustion **E**ngine
MEA	**M**ore **E**lectric **A**ircraft
MOSFET	**M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor
PCB	**P**rinted **C**ircuit **B**oard
PE	**P**ower **E**lectronics
PHEV	**P**lugin **H**ighbrid **E**lectric **V**ehicle
PSO	**P**article **S**warm **O**ptimization
RMS	**R**oot **M**ean **S**quare
SAF	**S**ustainable **A**viation **F**uel
SiC	**Si**licon **C**arbide
TDR	**T**ime **D**omain **R**eflectmetry
WBG	**W**ide **B**and**G**ap

WIPS **W**ind **I**ce **P**rotection **S**ystem

Physical Constants

Speed of Light	$c_0 = 2.997\,924\,58 \times 10^{8}\,\mathrm{m\,s^{-1}}$ (exact)
Vacuum permittivity	$\varepsilon_0 = 8.854\,187\,812\,8 \times 10^{-12}\,\mathrm{C\,V^{-1}\,m^{-1}}$
Vacuum permeability	$\mu_0 = 1.256\,637\,062\,12 \times 10^{-6}\,\mathrm{H\,m^{-1}}$
Elementary charge	$e = 1.602\,176\,634 \times 10^{-19}\,\mathrm{C}$

List of Symbols

C	capacitance	F
d	distance	m
f	frequency	Hz
G	conductance	S (Ω^{-1})
i	current in time domain	A
I	current in freq domain	A
	constant current	A
j	imaginary unit	
J	current density	$\mathrm{A\,m^{-2}}$
L	inductance	H
$\mathbb{N}$	set of natural numbers	
P	power	W ($\mathrm{J\,s^{-1}}$)
R	resistance	Ω
$\mathbb{R}$	set of real numbers	
t	time	s
v	voltage in time domain	V
V	voltage in freq domain	V
	constant voltage	V
W	Energy	J
ω	angular frequency	rad
Δ	error	%
α	aspect ratio	%

Chapter 1

Introduction

1.1 Social background around power electronics

The Paris Agreement [1] was adopted in 2015 as a countermeasure for global warming. Japan's CO_2 reduction target for 2030 is a 26% reduction from the fiscal 2013 level. In addition, the share of renewable energy in the total electricity generated by power sources is 16% in FY17, while the target for FY2030 is 22 – 24% (Fig. 1.1). Although the introduction of feed-in tariffs (FIT schemes) has reduced the price of renewable energy overseas, there are many issues that arise from the actual introduction of renewable energy. The Fifth Basic Energy Plan of the Ministry of Economy, Trade and Industry (METI) includes the promotion of low-cost renewable energy, overcoming grid constraints, and distributed energy as major measures [2]. Furthermore, for a long-term sustainable society, it is necessary to shift from fossil energy to renewable energy, and this trend will not be temporary but will continue in the long term (2050) [3].

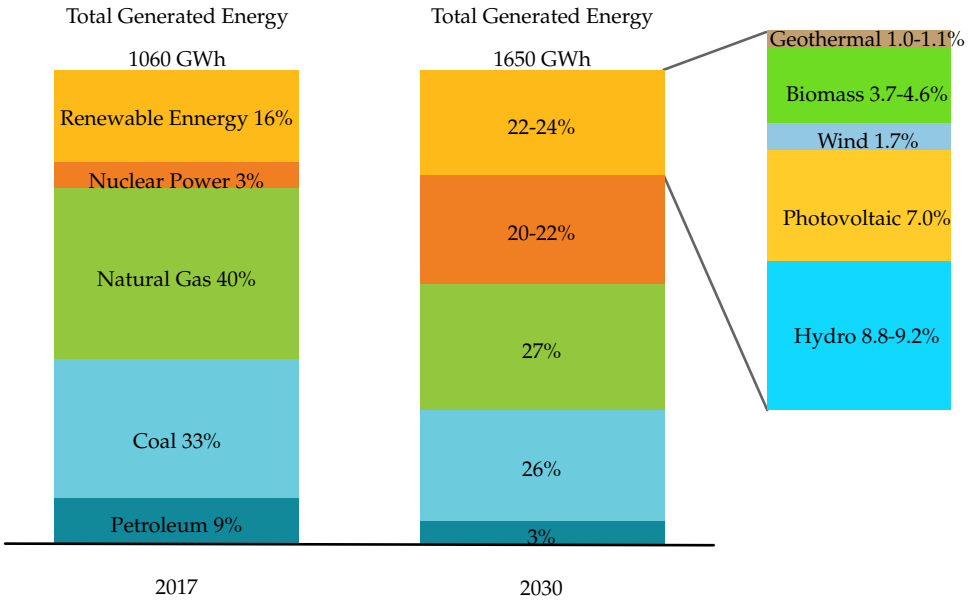


FIGURE 1.1: Breakdown of the energy supply in Japan [2].

Demand and supply of electricity must be in balance; if demand exceeds supply, the equipment cannot be used due to lack of necessary power, and if supply exceeds demand, energy overload must be handled strictly. Because power generation from renewable energy sources depends on the environment, it is difficult to predict the amount of power that will be generated, and even if power is generated, it may not be available, or it may not be generated when power is needed. For example, in mainland Kyushu, output control of solar power was implemented for the first time in 2018, and discussions are underway to fully utilize the benefits of solar power generation [4]. Therefore, the research, development, and diffusion of power electronics (hereafter referred to as "PE"), a technology for freely storing, transmitting, and consuming electrical energy, has become an urgent issue. In Japan, one of the goals is to develop a smart grid to solve these problems. A smart grid monitors the supply and demand of electricity at intermediate points in the power grid and optimizes the flow of electricity based on the calculated results. Therefore, the energy generated at each home or facility is not unstable when it is fed into the grid, and losses are minimized because the distance over which the power is transported is small. However, an energy storage system is also needed to store the energy generated by each power plant and renewable energy source, and a part of this energy storage system is the battery of the EV.

Figure 1.2 shows the forecast of electric vehicle sales based on the International Energy Agency survey [5]. The share of EVs is expected to be larger than that of PHEVs. Figure 1.3 depicts the ratio of greenhouse gas emissions that electric vehicles result in. ICEs and HEVs, whose main power source is fuel, emit the majority of their GHGs from fuel, while PHEVs and BEVs, whose main power source is the energy stored in their batteries, emit less than 50 percent of their GHGs from fuel. However, because of the large amount of GHG emissions from storing electric charge in the battery, the GHG emissions of BEVs, which do not use fuel for driving, are not significantly different from those of HEVs. Therefore, it can be said that the overall GHG emissions of BEVs can be reduced by using power generation methods that do not emit GHGs, such as renewable energy, to generate the electricity that is stored in the battery. Therefore, power generation from renewable energy sources and the widespread use of electric vehicles have a significant bearing on the reduction of greenhouse gas emissions.

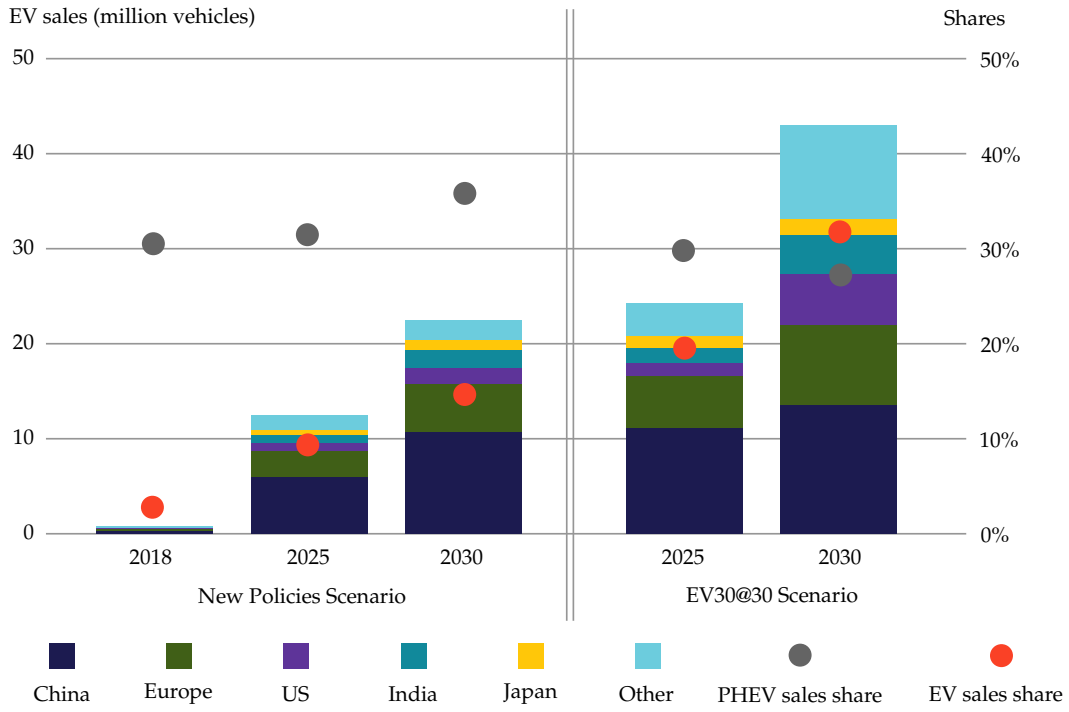


FIGURE 1.2: Projection of electric vehicle sales and share.

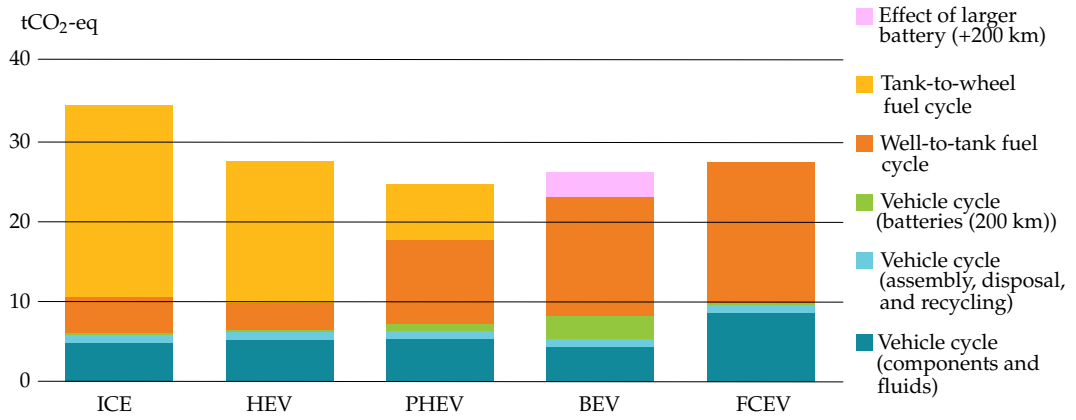


FIGURE 1.3: Ratio of the total energy for vehicles.

For them to be widely used in the future, EVs and devices such as power conditioners must be easy to use from the viewpoint of the consumer. For example, the power control unit (PCU) used in electric vehicles had a power density of 35 W/cc in 2014, and through research and development, a power density of 70 W/cc has been achieved so far. The power density is increasing year by year to improve fuel efficiency.

There is another example to reduce GHG emissions from the aviation point of view. Air Transport Action Group (ATAG) has released a report exploring the scenario to meet net-zero CO_2 emissions by 2050 [6].

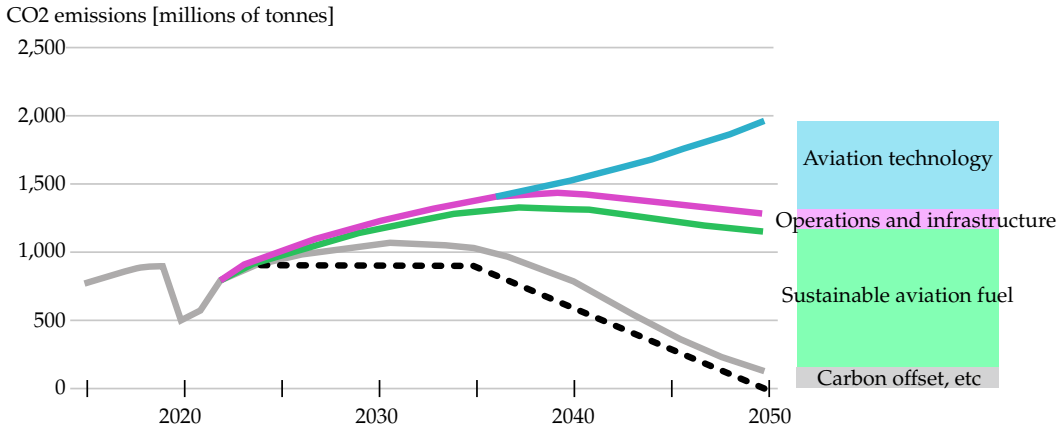


FIGURE 1.4: Net-zero carbon from aviation field[6].

Figure 1.4 displays the perspective CO_2 emissions with Scenario 1: pushing technology and operations. According to the report, aviation technology will reduce 12% of emissions reduction contributions by 2050, while the operations and infrastructure, and sustainable aviation fuel (SAF) reduce 9% and 71%, respectively. This

indicates that aircrafts such as drones, eVTOL, and civil airplanes must be operated with more and more high efficiency.

Table 1.1 shows the maximum motor output power for an electric aircraft [7]. The Maximum output power rises to 260 kW as of 2018 and the number of passengers are up to four. Additionally, the electricity for auxiliary units in electric aircrafts has several tens of kW to several hundreds of kW. Buticchi *et al.* [8] has reviewed the electricity generation and consumption in the on-board microgrids in the more electric aircraft (MEA). There are a lot of energy utilization (loads) in that system such as Wing Ice Protection System (WIPS), Electrical Environmental Control System (EECS), Electromechanical Actuators (EMAs), and Fuel Pumps (FP). These are summarized in Table 1.2. The number of these systems will increase when the scale of MEA increases and for further all electric aircraft. From these points, the demand of the power electronics circuits of around 10 kW to several hundreds kW must increase.

TABLE 1.1: Maximum motor output power

Year	2001–2010	2011–2015	2016–
Elec. Motor	– 92 kW	– 192 kW	– 260 kW

TABLE 1.2: Power consumption in the MEA

	Power [kW]
WIPS	40–60 and up to 200
EECS	– 70
EMAs	2–40
FP	200 kVA

1.2 Technical background

1.2.1 Trends of high power density converters

There are numerous studies that predict the efficiency of automotive and electrified airplanes [9]–[13]. The electrification of airplanes can increase the energy efficiency

from the batteries to motors, although there are inevitable issues. One is the reliability of the electric equipment and mechanical system since aircraft safety must be highly guaranteed [11]. Another issue is that the weight of the batteries and electric equipment may reduce the cruising distance when compared with conventional aircrafts. The required power weight density is 16.4 kW/kg according to the STARC-ABL Rev. B power system architecture designed by NASA [14]. Additionally, many researchers have reported on converters with high power weight density [15]–[30].

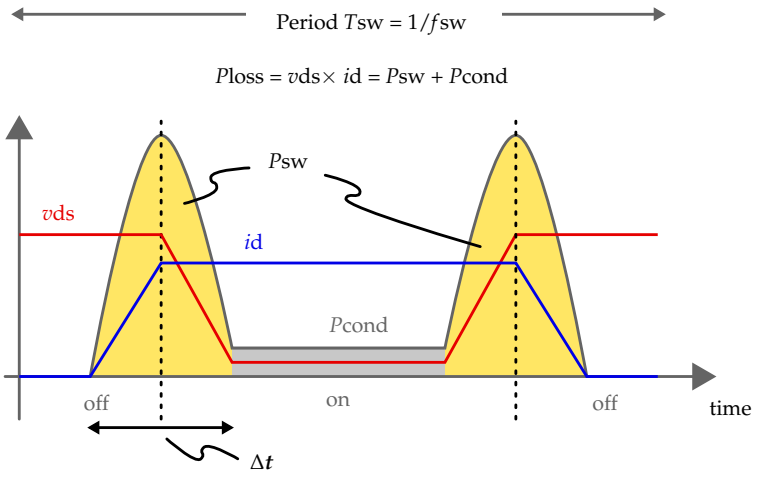
TABLE 1.3: Specifications of electrical components in STARC-ABL Rev. B [14]

Component	Power / Weight	Efficiency
Generator	13.2 kW/kg	96%
Motor	13.2 kW/kg	96%
Inverter	16.4 kW/kg	98%
Cable	3.9 kg/m	99.6%

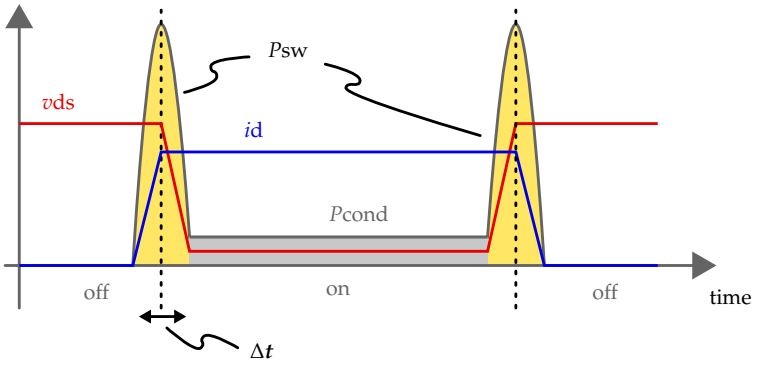
This concept was presented in 2017, and since then, the required power weight density has been increasing for further large-scale and electrified airplanes. Moreover, the voltage applied to the DC bus will be adopted in future aircraft over 1 kV to 3 kV. In such a system, the inverter technology has been developed using the power semiconductor devices. Recent wide-bandgap (WBG) power devices have a tremendous ability compared with conventional silicon devices [31]–[36]. One of the advantages of WBG devices is the high electron speed, which makes the speed of switching faster by approximately three times. This is called "High-Speed Switching," which can be applied to hard-switching inverters.

1.2.2 High-speed switching technology

The high-speed switching technology has been also investigated to reduce the losses in power devices [37]–[43].



(a) Normal switching waveforms



(b) High-speed switching

FIGURE 1.5: Switching waveform and switching loss.

Figure 1.5 shows the diagram of the power device waveforms and losses. At the off state, the power device has almost no loss. At the on state, there is a loss P_{cond} on the on-resistance of the device, which depends on the power device operating point and output current. Assuming that the load of the converter is inductive, higher power is consumed during the switching transition time Δt. The loss during switching transient is called switching loss P_{sw}. Since the switching loss occurs twice during the switching period, it is proportional to the switching frequency. Figure 1.5(b) depicts the high-speed switching compared with (a) normal switching. It is evident that the voltage and current derivative with respect to time is larger and hence, the switching loss P_{sw} is lower.

TABLE 1.4: Specifications of Nch Power MOSFET provided by Rohm

Product	Material	Voltage rating	Current rating	Rise time t_r	Fall time t_f
R6020PNJ	Si	600 V	20 A	60 ns	70 ns
SCT3120AL	SiC	600 V	21 A	21 ns	14 ns

Table 1.4 lists the switching speed of power devices from datasheet [44], [45]. This example shows that the SiC power device has three times or faster switching speeds than the Si device. The switching loss P_{sw} ideally reduces by three times in this example. The main advantages of high-speed switching are as follows:

1. Reduce the size of a cold plate (heatsink) because of the reduction in the loss
2. Increase the switching frequency f_{sw} by keeping the loss and thereby maintain the size of a cold plate

This dissertation targets the swithching speeds listed in Table 1.5.

TABLE 1.5: Target of switching speed in this dissertation.

device	turn-off transient time
Si-IGBT	100 ns - 400 ns
SiC MOSFET	10 ns - 100 ns

1.2.3 Issues of high-speed switching

Besides the advantages of high-speed switching, there are many issues that must be addressed [46].

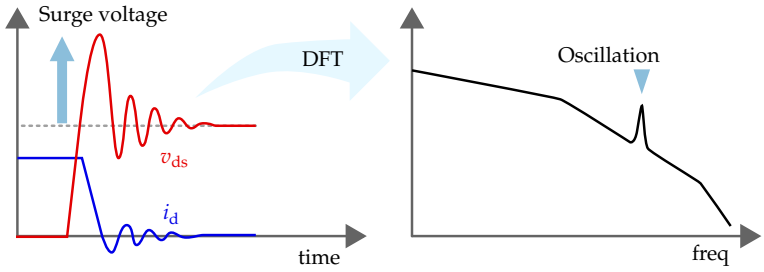


FIGURE 1.6: Issues caused by high-speed switching.

Figure 1.6 shows an overview of the issues reported with high-speed switching. As the switching speed increases, the time derivative of voltage and current (dv/dt and di/dt) increases. This results in higher noise generation understood by the voltage and current spectra derived from the Fourier transform of the waveforms. The

increase in the generation of high-frequency components results in noise issues [47]–[50]. The other issue is the voltage overshoot, which is the excess of the converter input voltage [51]–[53].

1.2.4 Parasitic parameters and high-speed switching

The issues of high-speed switching occur unexpectedly, even though the circuit designers construct the power electronics circuit. In most cases, the cause is parasitic parameters, which exist on every component in the circuit.

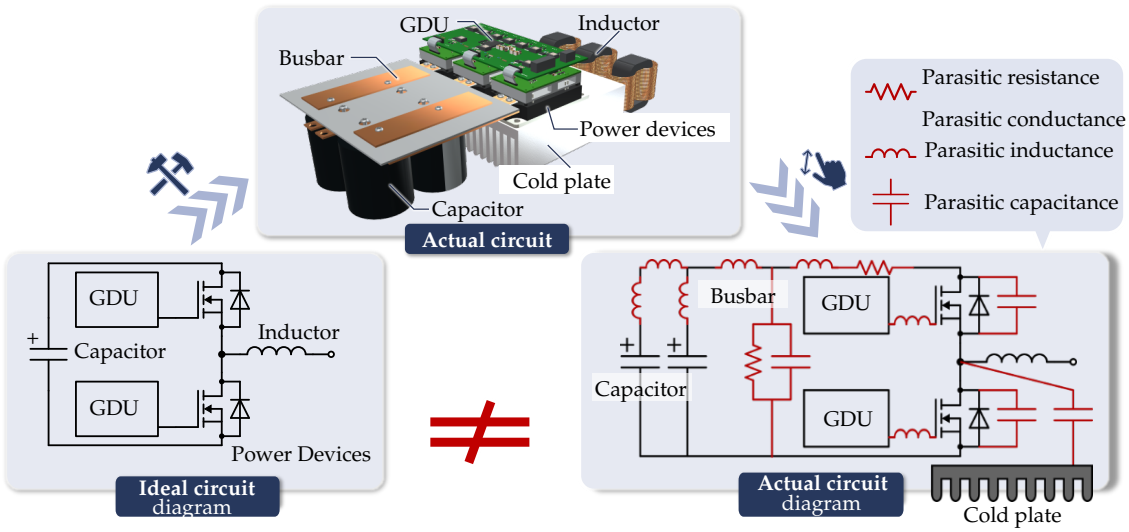


FIGURE 1.7: Differences between the ideal circuit and practical ciruits.

Figure 1.7 depicts the differences between the ideal (known as a textbook) and practical circuits. The ideal circuit includes only the passive components (capacitors and inductors) and power devices. The actual circuit is manufactured according to the ideal circuit. The practical circuit, however, includes parasitic parameters, multiple capacitors, cold plates on power devices, wirings (called "Busbar") for their connection, etc. The busbar is a metal bar (usually made of copper/aluminum) that connects the components electrically. The parasitic parameters are categorized into four; parasitic inductance, parasitic resistance, parasitic capacitance, and parasitic

conductance. These parameters impose the circuit operation, especially to the high-speed switching transient [54]. The parasitic inductance and time derivative of current $\mathrm{d}i/\mathrm{d}t$ invoke the voltage as shown in eq. 1.1.

$$v = L \times \frac{\mathrm{d}i}{\mathrm{d}t} \tag{1.1}$$

The parasitic capacitance and time derivative of voltage $\mathrm{d}v/\mathrm{d}t$ invoke the current as shown in eq. 1.2.

$$i = C \times \frac{\mathrm{d}v}{\mathrm{d}t} \tag{1.2}$$

For example, consider a converter rated at 500 V, 20 A, and transition time Δt of 10 ns; the voltage and current caused by $\mathrm{d}v/\mathrm{d}t$ and $\mathrm{d}i/\mathrm{d}t$ are dramatically large due to the high-speed switching, as shown in Table 1.6. This can be explained by Fig. 1.8.

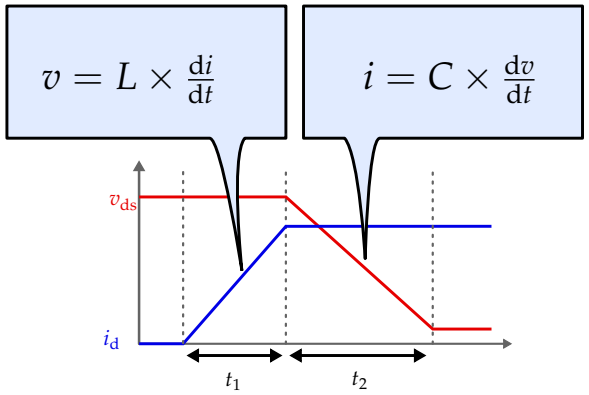


FIGURE 1.8: The voltage and current induced by the voltage and current derivatives of time.

For future converters, the switching speed increases more and more such that the increase in the invoked voltage and current is inevitable.

TABLE 1.6: The voltage and current invoked by the parasitic parameters and time derivative of current/voltage.

Voltage/current ratings	Transition time Δt	Parasitics	Time derivative	Invoked voltage/current
20 A	10 ns	50 nH	2 A/ns	100 V
500 V	10 ns	100 pF	50 V/ns	5 A

1.2.5 Parasitic parameters on the circuit components

Parasitic parameters exist on each component in converters. Figure 1.9 shows the categorization of the parasitic parameters on each component.

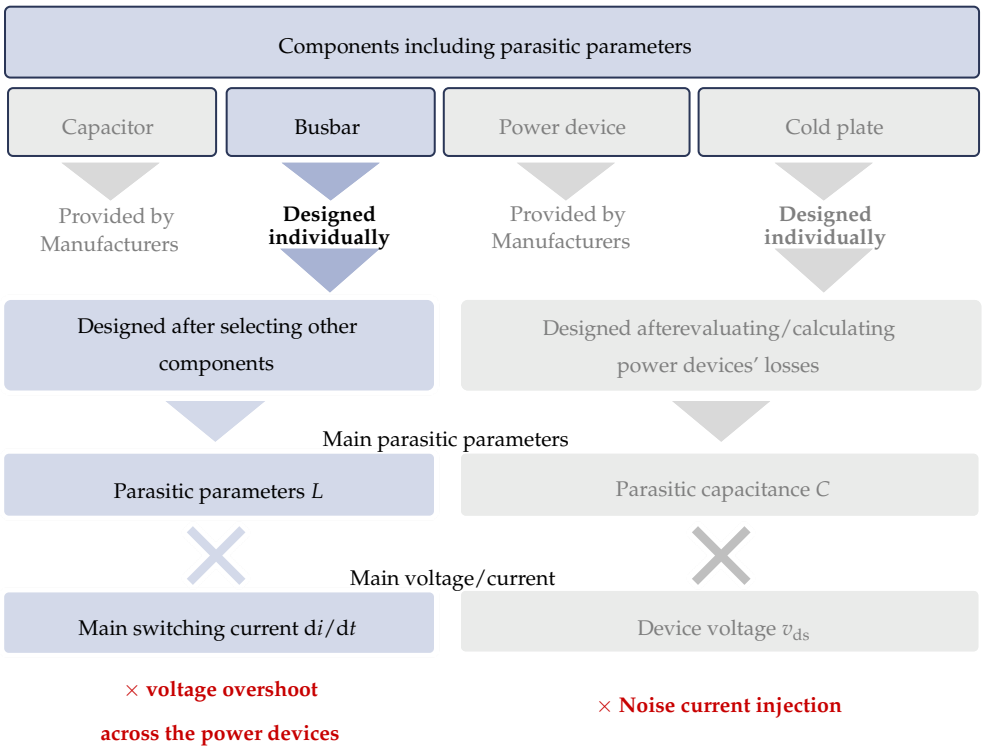


FIGURE 1.9: The main parasitic parameters on the components in the converter.

The main parasitics on the components are as follows. The capacitors have parasitic inductance, parasitic resistance, and parasitic conductance. The busbars have parasitic inductance, parasitic resistance, and parasitic capacitance. The power devices with a cold plate attached have parasitic inductance and parasitic capacitance [55]. Out of these components, the capacitors and power devices are provided as manufactured components, which the circuit designers cannot design inside these manufactured parts. This means that the circuit designers can just select the capacitors and power devices (though they can be designed by dedicated effort). Therefore, in this dissertation, the parasitic parameters in capacitors and power devices are assumed to be constant owing. On the other hand, the busbars and cold plates are designed individually after selecting the capacitors, power devices, etc. The cold plates are designed considering the heat dissipation of the power devices and the thermal management of the whole system. Because the cold plates have a heat

transfer function and not electron transfer, the parasitic parameters considered in the design is only parasitic capacitance. The busbar transfers the electrons from one component to the others; hence that the main current/voltage on the busbar is directly affected by the parasitic parameters.

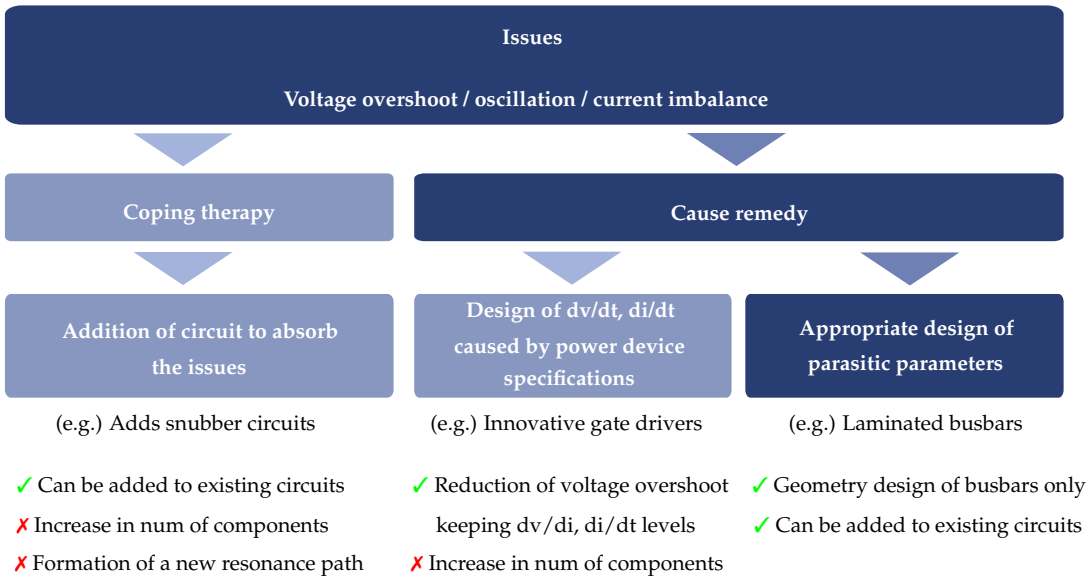


FIGURE 1.10: Coping therapy and cause remedy.

Figure 1.10 depicts the solutions to overcome the issues related to the parasitic parameters on the busbar. There are many ways to overcome these issues using coping therapy and cause remedy. For example, in coping therapy, addition of a sunbber circuit can absorb the voltage overshoot. However, this leads to increase in the number of components and formation of a new resonance path. Of course, the snubber circuit is actually effective; however, cause remendy will be a better solution for future power conversion circuits. Recent researches have proposed the use of innovative gate drivers that reduce voltage overshoot while maintaining the high-speed switching. However, it is difficult to implement the additional active gate drivers. To overcome the issues, an appropriate design of parasitic parameters, for exmaple, laminated busbars, is chosen. All that is required is to design the geometry of the laminated busbars. This is a simple solution compared to the others. However, ways to design the geometry of the laminated busbar is yet to be determined.

As the spectra of switching waveforms slide to the higher frequency, the parasitic capacitance and conductance on the busbar become crucial. Busbar-relevant

research has been published targetting such parasitic parameters. To avoid the parasitic parameters from affecting high-speed switching, it is desired to make the value of parasitic parameters to zero. It is of course impossible to perfectly eliminate the parasitic parameters. A few researchers have now achieved low parasitic parameters, such as low parasitic inductance, with busbar lamination.

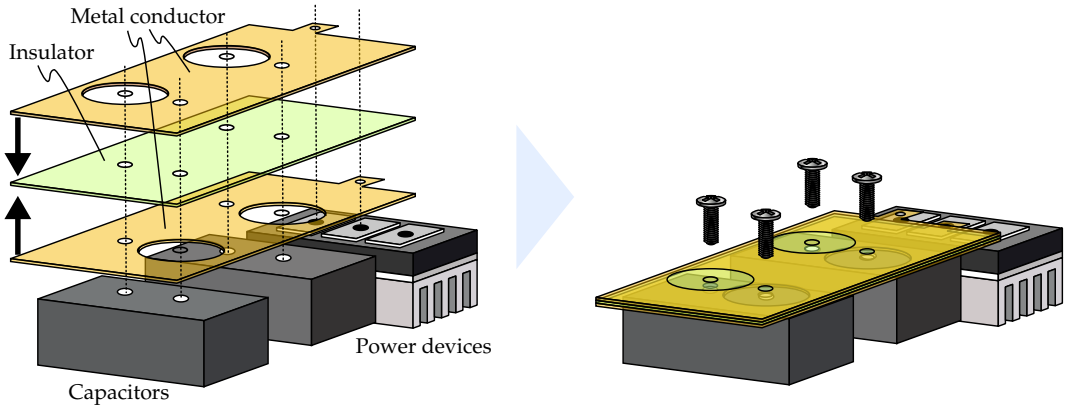


FIGURE 1.11: Structure of a laminated busbar.

Figure 1.11 depicts the structure of a laminated busbar. The positive and negative electrodes sandwich an isolation material, which result in low parasitic inductance because of flux cancellation.

1.2.6 Laminated busbar design for Power Conversion Circuits

A laminated busbar is basically designed to achieve low parasitic inductance. Figure 1.11 shows the laminated busbar model to analyze the parasitic inductance by electromagnetic (EM) simulation. It is to be noted that the laminated busbar is not as simple as just a bar. There are screws on the terminals, apertures for terminals, and other physical parameters, which affect the parasitic parameters. However, such a detailed profiles of the laminated busbar has not yet been considered. Instead, the laminated busbar has been analyzed by EM simulation after designing its structure. In this design scheme, if the specification of the designed converter is not acceptable for high-speed switching converter requirements, the converter must be redesigned. To satisfy the requirements of the high-speed switching converters, the parasitic parameters, which are the main cause of the issues, must be actively designed during the designing phase and not the evaluation phase.

1.3 Objective of this dissertation

This dissertation proposes the design method of a laminated busbar for high-speed switching converters. The proposed design methods are directed at the issues reported because of high-speed switching. Figure 1.12 shows the steps taken and the corresponding chapters.

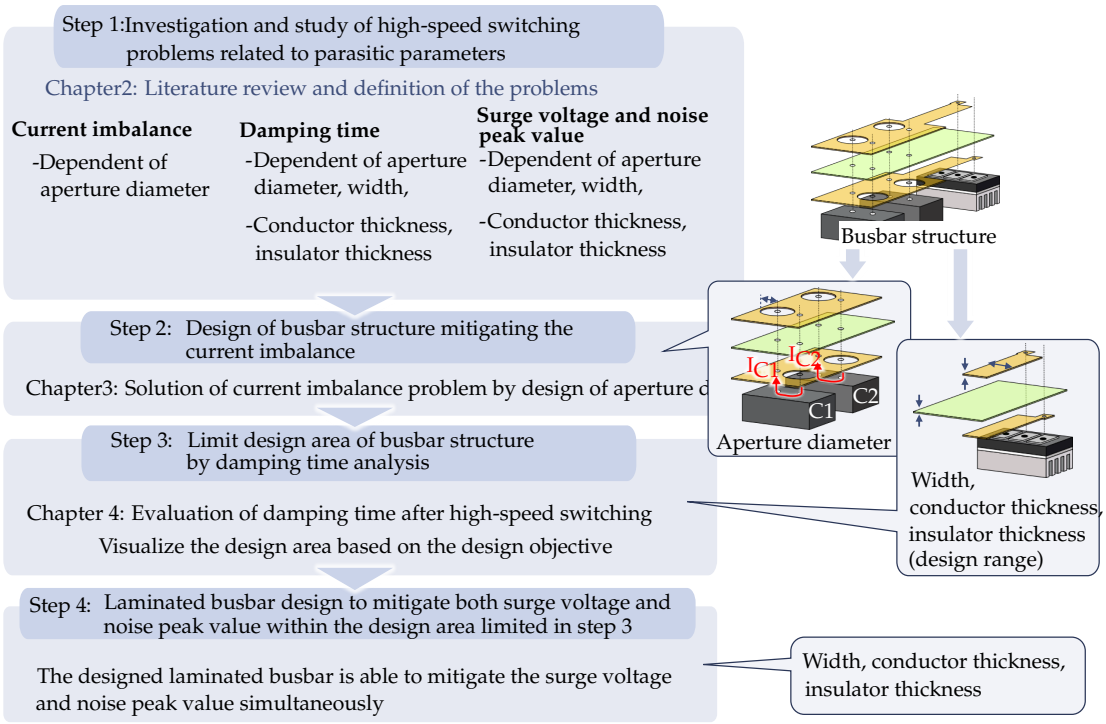


FIGURE 1.12: Dissertation outline and relationship between chapters.

1.4 Dissertation outline

This dissertation is structures as follows:

1 Indroduction

1.1 Social background around power electronics

1.2 Technical background

1.2.1 Trends of high power density converters

1.2.2 High-speed switching technology

1.2.3 Issues of high-speed switching

Chapter 2

Literature Review

This chapter summarizes the investigation of relevant papers on laminated busbar for high-speed switching and the issues of high-speed switching and parasitic parameters. The issues covered in this dissertation are defined to be addressed using the laminated busbar design method. In addition, the compartmentalization of this dissertation is clarified from the investigation. Figure 2.1 depicts the overview of this chapter. This chapter identifies problems with the current busbar design method and defines solutions through the following process.

1. Define the circuits and busbars covered in this dissertation
2. Clarify issues related to high-speed switching and laminated busbars
3. Investigate the relationship between parasitic parameters and laminated busbar geometry

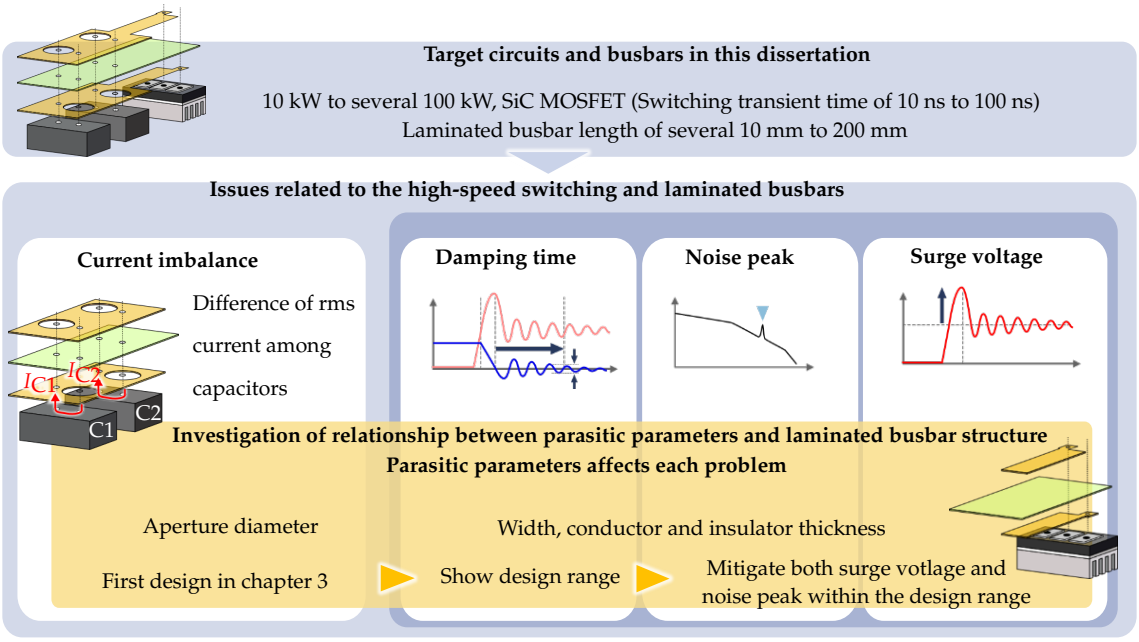


FIGURE 2.1: Outline and objective of this chapter.

2.1 Circuit and busbar scope of the dissertation

This thesis is concerned with power conversion circuits used in industrial, aerospace, automotive, and other applications described in Chapter 1. As such, voltage source converters with power ranging from 10 kW to several hundred kW are covered. In these applications, SiC MOSFETs have recently been applied for loss reduction and high-speed switching.

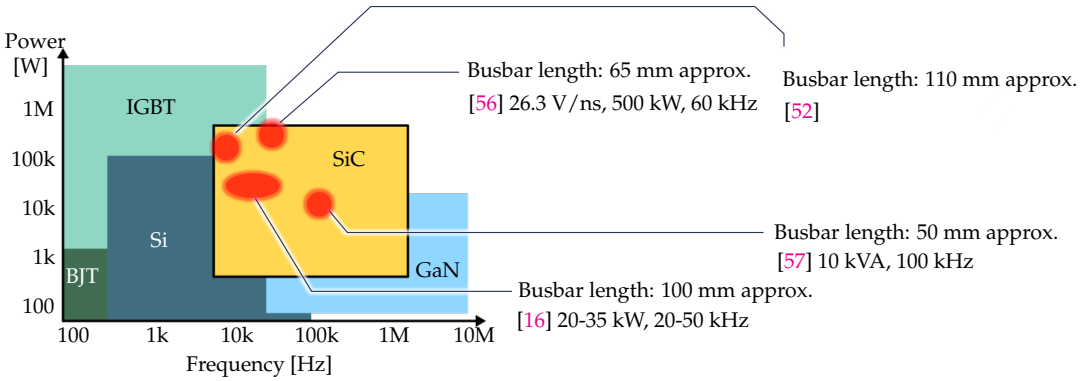


FIGURE 2.2: Circuit scope of the dissertation.

In the literature shown in Figure 2.2, switching speeds of 10 V/ns or higher have been experimentally verified.

In these power conversion circuits using laminated busbars, their length ranges from several tens to hundreds of millimeters. The switching speed of SiC is about several A/ns; therefore, the switching time is 10 ns or longer. The critical frequency at 10 ns is 15 MHz, and the corresponding wavelength is 18.8 m. Therefore, one-quarter wavelength is approximately 4.7 m, and the busbars discussed in this chapter can be applied to lumped passive components [58]. Most equivalent circuit of the laminated busbar is just inductance to simply consider the surge voltage. However, some papers have proposed a T-type lumped equivalent circuit using resistance, inductance, capacitance, and conductance. This T-type equivalent circuit is a strong candidate for equivalent circuits of a laminated busbar since it considers all losses in the busbars. The loss analysis has not been performed dedicatedly because the loss in the laminated busbar is quite small when compared with that of the power devices. There is also a Π-type equivalent circuit for the laminated busbar. Both types have advantages to consider each issue; therefore, this dissertation will use both the types depending on the issues to be addressed. To simplify the analysis, this dissertation concentrates on just one leg in the three phase inverters, which is same as buck chopper circuit configuration. Once the design of laminated busbars are validated for one leg cicuit configuration, it can be applied to three phases or more.

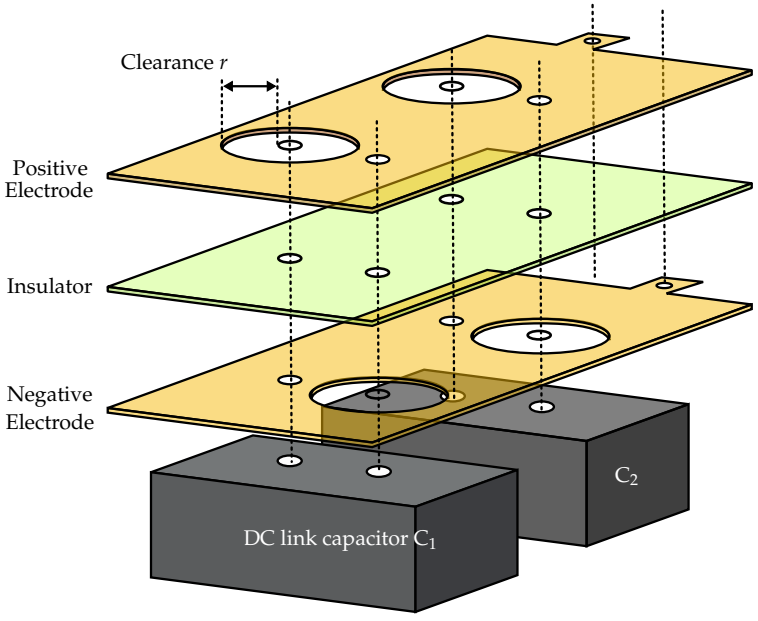


FIGURE 2.3: A 2-layer laminated busbar.

Before moving on to the detailed disccusion, we must review the layer structure of the laminated busbars. The most simple laminated busbar is a 2-layer conductor, as shown in Fig. 2.3. This simple structure enables the current path to be simply analyzed, easily manufactured and assembled, and has low weight. The biggest advantage of the 2-layer busbar is its heat transfer compared with three or more layers. Since the top and bottom layers touch the air for cooling directly, the thermal resistance is less.

A few other studies have proposed a 3-layer laminated busbar. Two of the three layers is the positive and negative electrode; third is the ground layer or mid-point layer, which is on the same net of output terminals or 0-voltage for 3-level NPC. The ground layer is used for good EMC performance [59], [60]. The 0-voltage net for 3-level NPC is used for achieving low inductance in the current commutation loop [61]–[63]. This current commutation loop includes the AC side busbar where the trapezoial voltage waveforms are applied.

There are papers describing 4- or more layer busbars as well. These papers adopted the multi level converters, which have many connections for the power devices. It is then inevitable to increase the number of layers for AC side busbars. A recent paper has proposed the multi-layer busbar to avoid the partial discharge for high-voltage applications [64].

TABLE 2.1: Review of the number of laminated busbar layers.

Num. of layers	Advantages	Refs.
1	Easy implementation	[65]
2	Easy implementation, Understandable relationship between the physical structure and electrical parameters, Low parasitic inductance	[37], [38], [59], [61], [66]–[77]
3	Low parasitic inductance, low CM noise	[59]–[63], [67], [78], [79]
4 or more	Low parasitic indutance, low stress of electric field	[59], [64], [77], [80]

Table 2.1 is the review of the layer consideration. The 2-layer laminated busbar is adopted in this dissertation owing to its various advantages.

2.2 Issues of high-speed switching

2.2.1 Current imbalance

A DC link capacitor is one of the passive componenets to be downsized to decouple DC bus side and switching device side. In general, there are two roles for a DC link capacitor. One is as a power buffer for the energy coming from the output power of converters; hence, an electrolytic capacitor is used in most cases [81]. Another role of DC link capacitor is for decoupling of switching components whose target is around/above switching frequency. For such a case, a capacitor bank, which is a set of capacitors in series and/or parallel, is frequently adopted to cover the voltage and current ratings of the converters [16]. There are several advantages on applying capacitor bank, such as lower parasitic inductance than that of a single capacitor that has the same total capacitance because of the parallel connection. For example, two film capacitors of EZPV60xxxMTB series (Panasonic) are listed in Table 2.2. It is evident that four 20 μF capacitors (EZPV60206MTB) (= 80 μF in parallel) has 6.875 nH, which is 79% less than the inductance 33.1 nH of a 80 μF capacitor (EZPV60806MTB). In addition, the root mean square (RMS) value of the permissible current is approximately twice higher.

TABLE 2.2: Parameters of capacitors EZPV60xxxMTB series.

Product number	Capacitance [μF]	ESL [nH]	ESR [mΩ]	Permissible current [Arms]
EZPV60206MTB	20	27.5	10.4	11.9
4 x EZPV60206MTB	80	6.9	2.6	52.1
EZPV60806MTB	80	33.1	3.9	24.3

Such a capacitor bank is assembled on a wiring on DC side of the converter. Thus, the wiring should be a wide plate to connect all capacitors, and their arrangement is important to ensure low parasitic inductance as well as the capacitor bank. The inductance of the wiring and capacitors is one of the issues of recent wide-band gap (WBG) devices operation. To consider the manufacturability, designability, and electrical specifications, a laminated busbar is one of the best solutions [64]. The terminals of capacitors are designed to avoid electrical breakdown with certain clearance. A design guideline specifies the profile for clearance, for instance, in IPC-2221.

Nowadays, this clearance is a critical parameter for medium/high voltage applications such as an aircraft DC bus of 3 kV [12]. For medium voltage applications, this clearance must be designed carefully because the electrical breakdown can cause failure of circuits and peripheral equipment [18].

There are various ways to avoid electrical breakdown; one possible solution is from material point of view. Another approach is a structure design of the busbar. The structure design of the busbar has advantages of simplicity, low cost, and flexibility. Ravi [64] proposed the design method of the conductor/insulator layout to ensure the electric fields for partial-discharge free operation. In such a structure design, circuit designers are able to pursue optimal impedance of busbars, which are parasitic parameters, by simply changing the design layout and keeping the electrical breakdown strength without material improvement even when there is a change in the design specification of applied voltage.

Regarding the busbar design, the parasitics, especially parasitic inductance, are minimized to suppress surge voltage [58]. The parasitic inductance between the DC link capacitors causes an LC resonant loop and increases the losses of the capacitors [56], [82]–[84]. This resonant phenomenon causes current imbalance within the capacitors and has a potential to degrade the capacitor rapidly whose rms value of current is the largest value among the cacpacitors [85]. The current imbalance within the capacitors increases as the parasitic inductance between the DC link capacitors increases. It is, however, inevitable to increase the clearance (apertures) for terminals of the busbars when applying the conventional (low/medium) circuit design to medium voltage applications. The parasitic inductane subsequently increases because the apertures on the busbar are on the way of a current commutation loop. There are few papers that discuss the relationship between the parasitic parameters and size of the clearance. Moreover, the resonance among the parasitic inductance of the busbar and DC link capacitors from an aspect of the busbar parasitics is yet to be studied.

As mentioned before, the current imbalance causes different rms values of current among the capacitors. Hence, this amount must be defined for quantitative evaluation. Let $I_{\mathrm{rms,max}}$ be the highest rms value of current and $I_{\mathrm{rms,min}}$ be the lowest

rms value of current. The difference is expressed as a percentage:

$$\Delta I = \frac{I_{\text{rms,max}} - I_{\text{rms,min}}}{I_{\text{rms,min}}} \tag{2.1}$$

This difference wears out and deteriorates the capacitors that has the highest current flow in comparison with the others.

2.2.2 Surge voltage

Fig. 2.4 shows a typical switching waveform under turn-off operation. The surge voltage V_{s} is evaluated because it may destroy the power device. This is due to high $\mathrm{d}i/\mathrm{d}t$, which induces a voltage between the stray inductances as electromagnetic force. The surge voltage and stray inductance can be related using the expression given:

$$V_{\text{s}} = -L_{\text{loop}} \frac{I_{\text{o}}}{t_2} \tag{2.2}$$

The surge voltage is mainly proportional to the total inductance in the commutation loop and the derivative of the drain current. Thus, the conventional busbar design promotes it to be wide and thin for low inductance. However, it is hard to numerically analyze the surge voltage when considering the device output capacitance and the busbar capacitance. Hayashi and Wada [86] reported that the surge voltage is affected by the loop inductance, common source inductance, and gate resistance. The common source inductance is present inside of the package of the power device. This study assumes that the capacitors and power devices are commercial products, while the busbars are designed. Thus, the parasitic inductance of the capacitors and power devices are constant in this study. Additionally, the gate resistance is the smallest possible constant value since the switching speed needs to be high. In chapter 5, the gate resistor design is also presented to guarantee the proposed laminated busbar design method, while this gate resistor design must be the last resort.

Figure 2.4 shows the turn-off waveforms of drain-source voltage and drain current. The surge voltage occurs during t_2 term since the current falls from the output

current to zero and has the derivative of time. During this term, the voltage is actually not a constant value as described in eq. (2.2). This is because of the current derivative of time, which is not a constant value. In addition, the current begins to oscillate at the start of t_2. The voltage during t_2 also oscillates owing to the current oscillation. As the result, it will be challenging to detect the maximum voltage. Because of these reasons, in this study, the surge voltage is defined as the maximum point of v_{ds}, and this is seen during t_2 in Fig. 2.4.

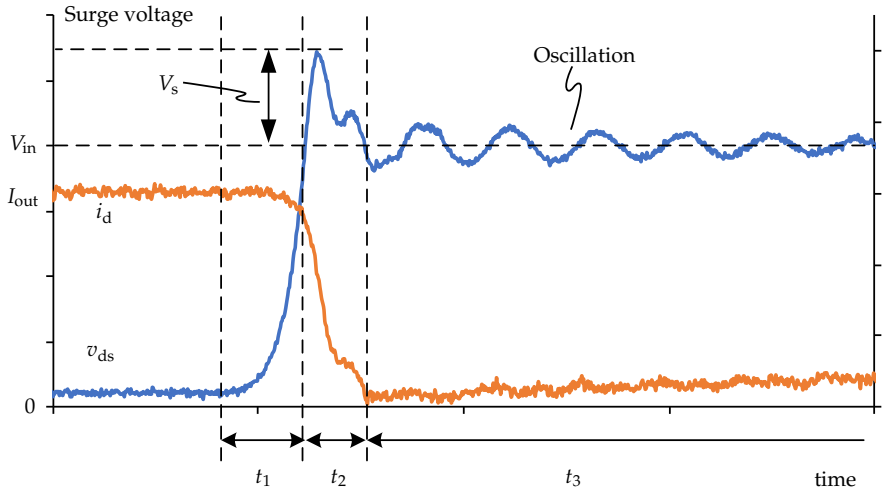


FIGURE 2.4: Surge voltage waveform.

2.2.3 Damped oscillation

Damped oscillation can be observed after the power devices switching, as shown in Fig. 2.4. When the MOSFET turns off, parasitic inductance, capacitance, and resistance forms a resonant circuit in the converter circuit. The pulse current and voltage generated in the power devices stimulate the resonant circuit, leading to the oscillation of the drain current i_d and drain-source voltage v_{ds}. It can be observed that the damped oscillation level becomes high when the parasitic capacitance of the bus bar and output capacitance of MOSFET are relatively large. The resonant frequency of the damped oscillation is determined as f_r by parasitic parameters, including the bus bar. Then, the derivative of drain current di_d/dt is one of the components that decides the amplitude of oscillation of voltage v_{ds}. In addition, the spectrum at the resonant frequency becomes larger as di/dt increases when applying high-speed

switching devices. Thus, the gate resistor also affects the damping oscillation because it can control the switching speed.

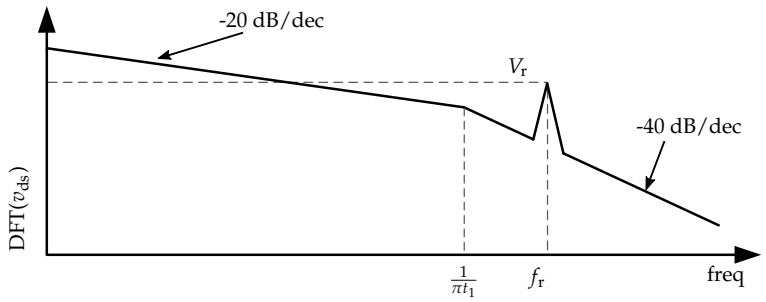


FIGURE 2.5: An example in the spectra envelope of trapezoidal switching waveform of v_{ds}.

Fig. 2.5 shows one example in the spectra envelope of the switching waveform v_{ds} that has damped oscillation after devices switching. The spectrum is calculated by using the discrete Fourier transform (DFT). Assuming that the switching waveform is trapezoidal, the magnitude of the spectrum decreases by 20 dB/dec till $1/\pi t_1$, and then decreases by 40 dB/dec [50]. Besides, the spectrum has a peak value at the frequency f_r if the trapezoidal waveform has damped oscillation. The peak value has a major effect in terms of electromagnetic interference; this peak value V_r of the discrete Fourier transform of v_{ds} is considered as one of the parameters to evaluate the switching waveform. Many papers concentrate on the evaluation of the damped oscillation level in the frequency domain and do not focus on the detailed characteristics of the damped oscillation in the time domain. However, the oscillation in time domain may interfere the communication signal based on the send/receive timing [87]. In addition, the current to be sensed on the DC side will fail if the oscillation is not damped enough. Such current sensing on the DC side is used to reduce the current sensors, and researches related to this technique is widely performed [88], [89]. Therefore, the oscillation caused by high-speed switching must be handled in the time domain as well. In this dissertation, the time is evaluated from the time of MOSFET switching till the oscillation amplitude is damped at a certain level.

2.3 Laminated busbar and parasitic parameters

Since the parasitic parameters of the laminated busbar depends on its structure, the relationship between the parasitic parameters and laminated busbar strucutre has been investigated by many researchers. This section summarizes this relationship and discusses the equivalent circuit of the busbar that is suitable for this study.

2.3.1 Parasitic inductance

The flux generated by the current is the principle of parasitic inductance is the flux generated by current. All components have parasitic inductance with non-zero value because there is current in each component. The magnetic field strength $\mathbb{H}$ generated by current $\mathbb{I}$ is expressed as follows:

$$\mathbf{H} = \frac{\mathbf{I} \times \mathbf{r}}{2\pi r^2} \tag{2.3}$$

The magnetic field strength can be transformed to the magnetic flux.

$$\mu \oint \mathbf{H} d\mathbf{S} = \Phi \tag{2.4}$$

The current I and flux Φ generated by the current has a proportional relationship.

$$\Phi = L\,|\mathbf{I}| \tag{2.5}$$

where L is the inductance. From these equations, it is evident that the constant coefficient of L depends on where the current and magnetic flux flow. Normally, busbars consist of the copper and oiled paper or ceramics, and hence, the magnetic flux path can be considered as a vaccum case. This implies that the inductance L depends on only the current path in this case, which is the conductor structure of a laminated busbar.

Schanen *et al.* [66] proposed the calculation of the parasitic inductance on a 2-layer laminated busbar. The calculation is based on self inductance and mutual inductance. The mutual inductance has a negative value since the current flows in opposite directions in the positive and negative electrodes. The conductors are divided

into many partial pipes and all of them have self and mutual inductances. The precise value of parasitic inductance can then be achieved. To decrease the inductance, the negative term, that is, the mutual inductance, must be maximized. This means that the lamination area should be enlarged and the insulation thickness should be decreased.

Recent papers concentrate on the inductance of the laminated busbar related to its terminal geometry. Wang *et al.* [72] investigated the relationship between the apertures on the laminated busbar and parasitic inductance. The apertures are holes on the conductors to connect the capacitors and power devices to the busbar. As the diameter of apertures increases, the parasitic inductance increases. Xu *et al.* [61] have shown the relationship between the distance between the terminals and parasitic inductance. The inductance increases as the distance of the terminals increases. The aperture is made by removing the conductor as a round shape while the distance of terminals does not change the area of the conductor. Therefore, the aperture size and distance of the terminals are also designed quantatively and covered in this dissertation.

2.3.2 Parasitic capacitance

The parasitic capacitance exists between the positive and negative electrodes. The capacitance is expressed as follows:

$$C_{\text{bus}} = \varepsilon_0 \dot{\varepsilon_{\text{r}}} \frac{S}{d} \tag{2.6}$$

where ε_0 is the vaccum permittivity, $\dot{\varepsilon_{\text{r}}}$ is the complex relative permittivity, S is the area of the conductor, and d is the thickness of the insulator. It is easy to understand that the capacitance of the laminated busbar is calculated using the geometric parameters such as thickness of the insulator. Hino and Wada [90] has proposed the calculation of the capacitance sweeping the geometric parameters. Figure 2.6 shows the relationship between the capacitance of the laminated busbar and its geometry. The capacitance can be reduced by reducing the length of the busbar. In addition, increasing the insulator thickness reduces the capacitance; however, the inductance

must increase as discussed previously. Thus, the capacitance and inductance is in a trade-off relationship and must be carefully designed.

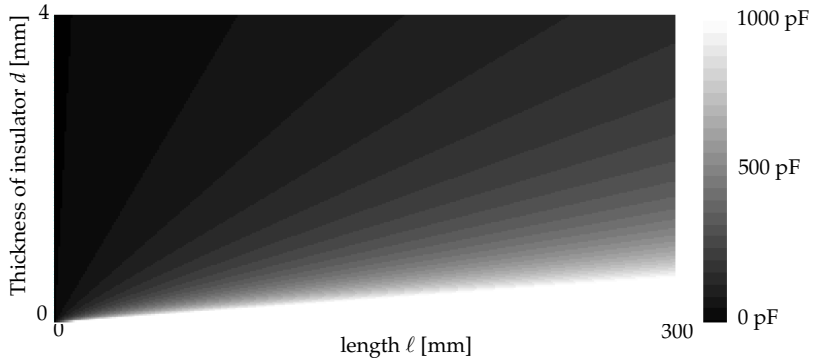


FIGURE 2.6: Capacitance map.

2.3.3 Parasitic resistance

The parasitic resistance has 2 categories: one is the DC resistance and the other is the AC resistance.

As the frequency of the current flowing in a conductor increases, the current density in the cross-section of the conductor is not uniform, but is concentrated on the conductor surface and corners, resulting in an increase in the resistance of the conductor. This phenomenon is called the skin effect, where the current concentrates on the surface from the conductor surface to the skin depth expressed by eq. (2.7).

$$\delta = \sqrt{\frac{2}{\omega\mu\sigma}} \tag{2.7}$$

In general, the skin depth equation is theoretically applicable to a single circular conductor, and approximations are needed to apply it to other conductor geometries.

When charge (current) flows through one conductor, the charge flowing through another conductor is attracted to it by the Lorentz force, resulting in the current being biased toward the inside of the two conductors and increasing the resistance. This phenomenon is called proximity effect. Another understanding of the proximity effect can be explained using eddy currents as well as skin effect. The eddy currents are stimulated by the currents flowing in conductors facing each other in opposite directions. This means that the single conductor does not produce proximity effect

[91]. Dowell [92] proposed an approximate formula for transformer windings, and literature [93] for laminated bus bars.

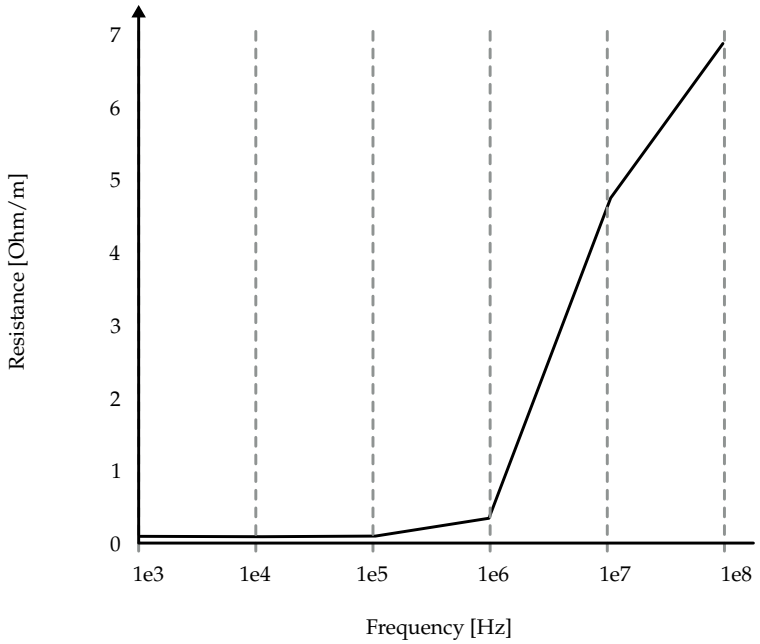


FIGURE 2.7: Resistance in simulation with skin effect [93].

Figure 2.7 compares the measured and approximate calculated values in Ref. [93]. It is confirmed that the measured and approximate calculated values agree in terms of the frequency range, geometry, and number of sample points. When the frequency of the voltage and current is several MHz, this resistance value of several ohms is applied.

2.3.4 Parasitic conductance

The insulation material has a complex permittivity that leads to dielectric loss. The complex permittivity is expressed as follows:

$$\dot{\varepsilon}_r = \varepsilon' - j\varepsilon'' \tag{2.8}$$

$$\tan D = \frac{\varepsilon''}{\varepsilon'} \tag{2.9}$$

where $\tan D$ is the tangent delta and ε' is the real part of the permittivity. This produces the real part in the admittance as shown below:

$$Y = \omega\varepsilon_0\varepsilon''\frac{S}{d} + j\omega\varepsilon_0\varepsilon'\frac{S}{d} \tag{2.10}$$

The real part is known as conductance in general. Depending on the insulation material of the laminated busbar, the conductance may not be ignored. For example, recent laminated busbars are made using printed circuit boards with the insulation material of FR-4. The high-speed switching waveform indudes the high frequency component, and so the parasitic conductance may be a crucial component to be considered. In general, the dielectric loss dramatically increases over GHz range, which are not targeted by the power conversion circuits. Djordjevic *et al.* [94] has reported that tan D increases in the MHz range though. However, most papers have ignored the parasitic conductance in the laminated busbar design although they refered to parasitic conductance since the parasitic conductance has less influence [68]. Compared with the switching loss, the dielectric loss is less than 1% in the simple calculation (several hundreds of mW to several watts).

In other words, the dielectric loss may have a potential to dampen the parasitic oscillation caused by the high-speed switching. This is because the energy stored in the oscillation is at the same level as that of the dielectric loss and the frequency is over several tens of mega hertz. Thus, the dielectric loss will be considered only for the oscillation term in this study.

2.4 Design consideration

From the discussions above, the parasitic parameters affects the each problem. If the surge voltage is mitigated to make a thin laminated busbar, the noise peak will be large. There is a trade-off relationship between the parasitic parameters and problems. Hence, the busbar is divided into two sections as shown in Fig. 2.8. It is evident that the aperture diameter affects all the problems, but the width and thickness does not affcect the current imbalance problem. Thus, the first design is directed toward current imbalance mitigation with the design of aperture diameter. After the design of aperture diameter, the capacitor bank with the busbar in capacitor side can be treated as a single capacitor. In chapter 4, design of the damping time is discussed, which combination of the single capacitor and busbar on the device side. The damping time must be mitigated within the design objective; otherwise, the control

of the circuit will be lost. Chapter 4 will explain the design range, where the damping time is designed within the objective value. After the design of damping time, surge voltage and noise peak are mitigated by the laminated busbar structure in the design range. These two problems are as good as small; hence, they are designed simultaneously. This procedure is summarized in Table. 2.3.

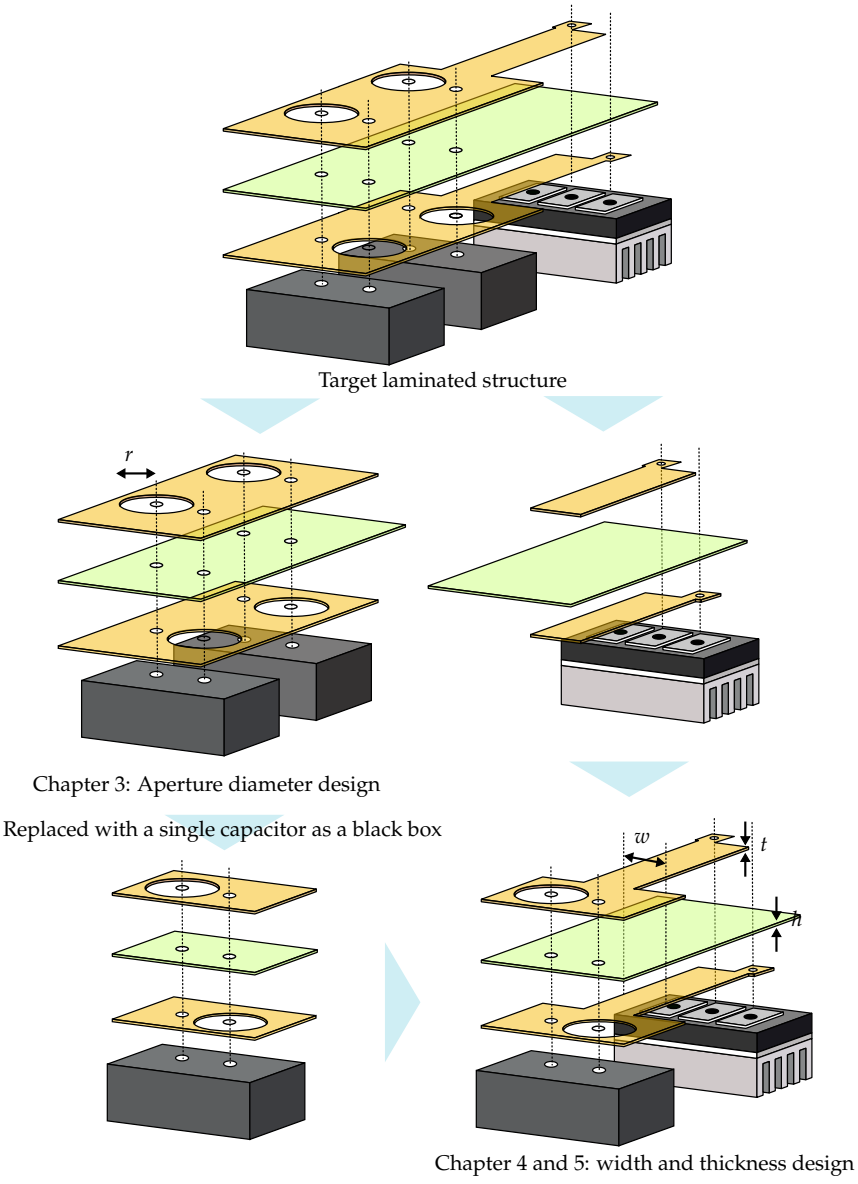


FIGURE 2.8: Target busbar structure and design strategy.

TABLE 2.3: Design procedure.

Design procedure	Chapter	Problems	Busbar structure
Step 1	Ch. 3	Current imbalance	Aperture diameter
Step 2	Ch. 4	Damping time	Width, conductor and insulator thickness (show design range)
Step 3	Ch. 5	Surge voltage and noise peak	Width, conductor and insulator thickness

2.5 Summary

Figure 2.9 depicts the summary of this chapter. The issues related to high-speed switching are defined to be handled quantitatively. To consider the relationship between parasitic parameters and laminated busbar structure, all the parasitic parameters of inductance, capacitance, resistance, and conductance must be designed simultaneously. Otherwise, the design to overcome an issue will worsen the other issues because parasitic parameters are in a trade-off relationship. The key to design the parasitic paramters is, of course, by reducing the parasitic inductance, and utilizing the parasitic capacitance as a low value and selecting proper resistance and conductance to decay the oscillation by considering their frequency characteristics.

Issues related to high-speed switching			
	Current imbalance	Oscillation	Surge voltage
Definition	difference of rms current in each capacitor	Oscillation waveform - frequency domain: Peak value at resonant frequency - time domain: time to decay to a certain value	Maximum drain-source voltage
Critical parasitic parameters	Parasitic resistance Parasitic inductance	Parasitic resistance Parasitic inductance Parasitic conductance Parasitic capacitance	Parasitic inductance

Parasitic parameters and geometry of a laminated busbar				
	R	L	G	C
Insulator thickness increase ↗ decrease ↘	depends	↗ ↘	↘ ↗	↘ ↗
Conductor width increase ↗ decrease ↘ * keep the cross-section area	depends	↘ ↗	↗ ↘	↗ ↘
Aperture diameter increase ↗ decrease ↘	↗ ↘	↗ ↘	→ ↗	→ ↗
Distance between terminals increase ↗ decrease ↘	↗ ↘	↗ ↘	— —	— —

FIGURE 2.9: Summary of chapter 2.

Chapter 3

Impact of Aperture Size on a Laminated Busbar to Current Imbalance Ratio among DC Link Capacitors

This chapter proposes a design procedure for laminated- busbar apertures, and holes on the busbar for assembly and electrical clearance by considering the current imbalance among the DC link capacitors. In addition, this chapter deals with the analysis of parasitic parameters on the busbars considering the aperture size. The proposed analysis reveals the current imbalance phenomena among the DC-link capacitors for the high-frequency operation of power conversion circuits. This chapter targets the isolation design for medium voltage applications such as converters in aircrafts, and the high-speed switching of power devices from the point of view of power density. Hence, the size of the apertures should be designed from both aspects of isolation and parasitic parameters. It is shown that the parasitic inductance and resistance of the laminated busbar increase due to apertures on the other side of the laminated conductor. The electromagnetic simulation displays the imbalance of the inductance and resistance that causes the current imbalance. When the aperture size increases from 20 mm to 50 mm, the imbalance of inductance and resistance increases by 392% and 302%, respectively. Additionally, theoretical analysis reveals the relationship between the current imbalance ratio and the size of the apertures to

consider the appropriate switching frequency. In the experimentation section, the current compensation method for the shunt resistor using convolution analysis is demonstrated, while high-frequency current sensing has been identified as a challenge in the wide laminated busbar. The experimentation validates the proposed procedure using buck converter circuits, rated at 500 V and 20 A. At a switching frequency of 666 kHz, it is confirmed that the current imbalance ratio is 35.9%.

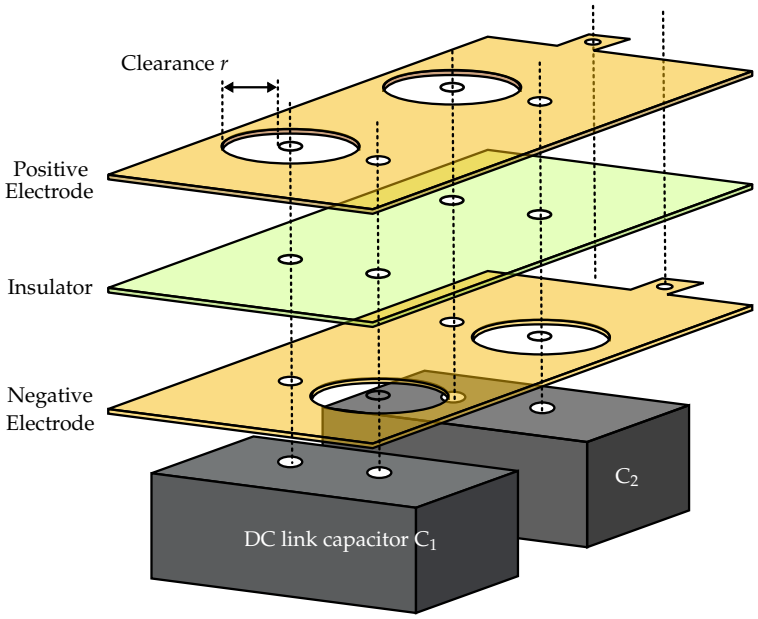
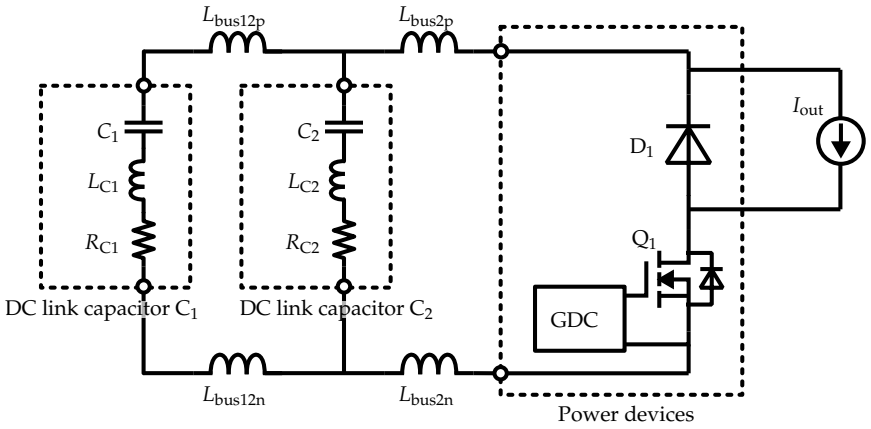
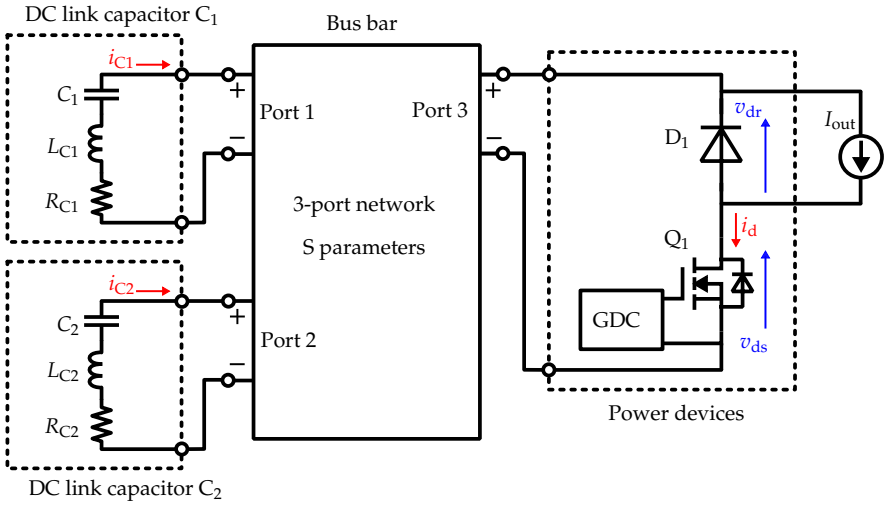


FIGURE 3.1: Laminated busbar structure with two capacitors.

3.1 A laminated busbar with apertures



(a) Conventional circuit diagram with the busbar inductance.



(b) Busbar model of S-parameters.

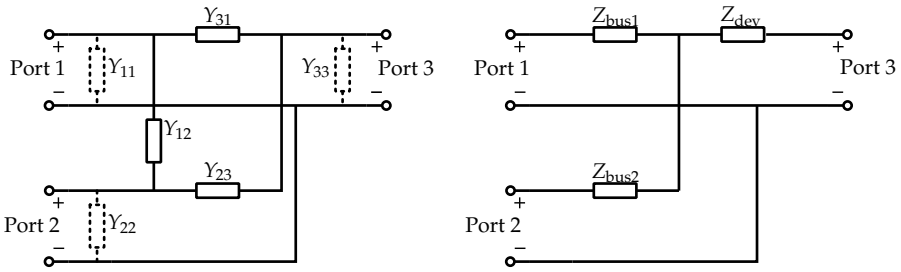
FIGURE 3.2: Buck converter circuit with 2 capacitors and a busbar.

3.1.1 Laminated busbar model

Fig. 3.1 shows a laminated busbar structure with DC link capacitors. The upper conductor is the positive electrode and the lower conductor is the negative electrode, and insulation material is sandwitched between them. The positive and negative terminals of the DC link capacitor are respectively connected to the positive and negative electrodes. At those points of connection, there are apertures for the terminals with certain clearance to avoid electrical breakdown.

Fig. 3.2 is a circuit diagram of a buck converter with the busbar and two DC link capacitors, C_1 and C_2. In the conventional method, Fig. 3.2(a) considers the

busbar inductance denoted as L_{bus12p} and L_{bus12n} between C_1 and C_2, and L_{bus2p} and L_{bus2n} between C_2 and the power device [95]. It is simply understandable to model the busbar as shown in Fig. 3.2(a), but this model can consider only the busbar geometry and the arrangement of capacitors as shown in Fig. 3.1. To cover any arrangement of the capacitors on the busbar, a circuit diagram with a busbar model of a 3-port network is proposed and shown in Fig. 3.2 (b). Since the busbar has three ports for DC link capacitors and a power device in this case, it is expressed as a 3-port network in general. This model does not include the physical placement of each port, which is the advantage to consider the parasitics generally. These busbar parasitics can be extracted from EM simulation [96].



(a) Y-type 3-port network equivalent circuit (b) Δ-Y transformed equivalent circuit

FIGURE 3.3: Equivalent circuit of the busbar with a 3-port network.

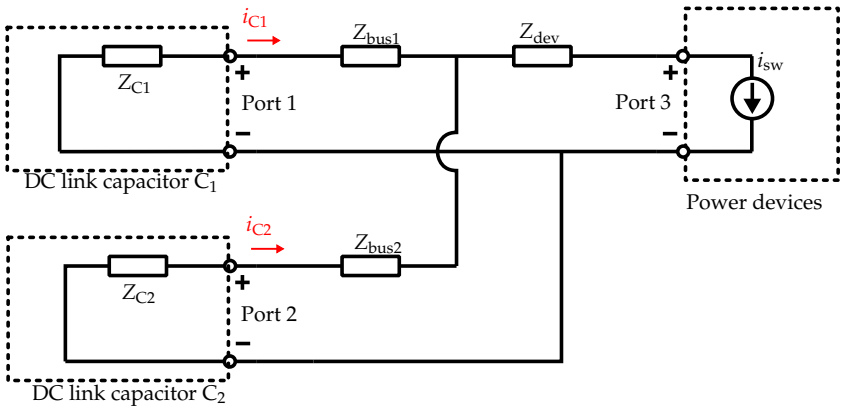


FIGURE 3.4: Equivalent Circuit of Fig. 3.2.

Fig. 3.3 shows the equivalent circuit of the busbar with a 3-port network. The conductance Y_{ij} $(i, j \in \mathbb{N})$ can be calculated from Y-parameters, which are transformed from S-parameters that are the results of EM simulation. The variable Y_{ii} represents the capacitance and conductance of the busbar. Normally, these parameters relate to high-frequency ringing above 10 MHz [97]. This study focuses on the current imbalance caused by resonant phenomena but for such ringing; thus, Y_{ii}

is ignored in this study. Then, the Π-type equivalent circuit of Fig. 3.3(a) is transformed as shown in Fig. 3.3(b), where Z_{bus1}, Z_{bus2}, and Z_{dev} are the impedances of the busbar. Z_{dev} is also ignored in this study since it exists on the current source side and does not affect the current imbalance analysis. On applying this equivalent circuit of the busbar to the circuit diagram in Fig. 3.2, the equivalent circuit in Fig. 3.4 is obtained. Each impedance has its parasitic parameters and are defined as follows:

$$Z_{\text{bus1}} = R_{\text{bus1}} + j\omega L_{\text{bus1}} \tag{3.1}$$

$$Z_{\text{bus2}} = R_{\text{bus2}} + j\omega L_{\text{bus2}} \tag{3.2}$$

$$Z_{\text{C1}} = R_{\text{C1}} + j\omega L_{\text{C1}} + \frac{1}{j\omega C_1} \tag{3.3}$$

$$Z_{\text{C2}} = R_{\text{C2}} + j\omega L_{\text{C2}} + \frac{1}{j\omega C_2} \tag{3.4}$$

where $Z_{\text{C}x}$ ($x \in \{1,2\}$) is the impedance of the DC link capacitors, and $R_{\text{bus}x}$ and $L_{\text{bus}x}$ are the parasitic resistance and inductance, respectively. $Z_{\text{bus}x}$ depends on the busbar structure and as a result, the size of the apertures r. Fig. 3.5 depicts the trapezoidal current source i_{sw}, which is equal to the DC side current of the buck chopper circuit.

$$i_{\text{sw}} = \begin{cases} Dt - \frac{I_{\text{out}}}{2} & \text{(a)} \\ \frac{I_{\text{out}}}{2} & \text{(b)} \\ -D(t - T/2) + \frac{I_{\text{out}}}{2} & \text{(c)} \\ \frac{-I_{\text{out}}}{2} & \text{(d)} \end{cases} \tag{3.5}$$

$$D = \frac{I_{\text{out}}}{\Delta t} \tag{3.6}$$

It should be noted that i_{sw} starts at time = 0, as shown in Fig. 3.5, where T is a period equal to the inverse of f_{sw}.

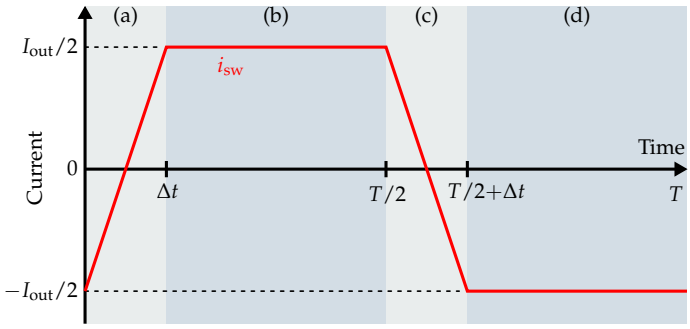
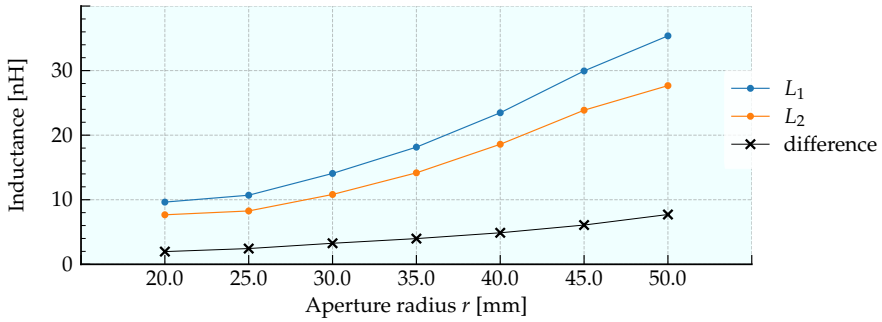


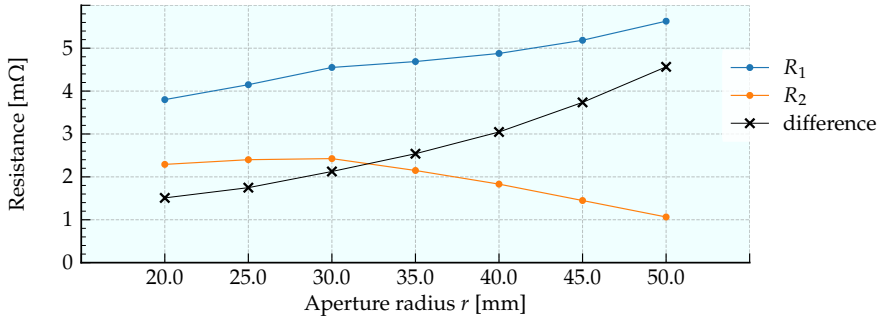
FIGURE 3.5: Switching waveform of current i_{sw} in Fig. 3.4.

3.1.2 Parasitic parameters and aperture size

The EM simulation or calculation is practically used [98] to extract the parasitic parameters. This study utilizes the EM simulator, Pathwave Advanced Design System (ADS, Keysight Technologies, Santa Rosa, CA, +1). ADS supports the Finite Element Method (FEM) in solving Maxwell's Equations. After solving the fields, the simulator calculates the S-parameters.



(a) Parasitic inductance.



(b) Parasitic resistance.

FIGURE 3.6: Parasitic parameters of the busbar at 100 kHz.

Fig. 3.6 shows the EM simulation results of parasitic parameters. In Fig. 3.6(a), the inductance increases as the aperture size r increases. In addition, the difference between L_{bus1} and L_{bus2} becomes 3.92 times higher at r = 50 mm than that at r = 20

mm. In Fig. 3.6(b), the resistance seems to decrease as the aperture size r increases. However, the resistance R_{dev} increases instead, thereby raising the total resistance. Furthermore, the difference between R_{bus1} and R_{bus2} becomes 3.02 times higher at r = 50 mm than that at r = 20 mm; similar is the case with inductance. In both cases of inductance and resistance, the difference gets wider as the aperture size increases. It is assumed that the aperture size of C_2 is on the path of the current coming from C_1. In the next section, it is shown that these difference affects the current imbalance, resulting in a large current imbalance in the case of a large aperture size.

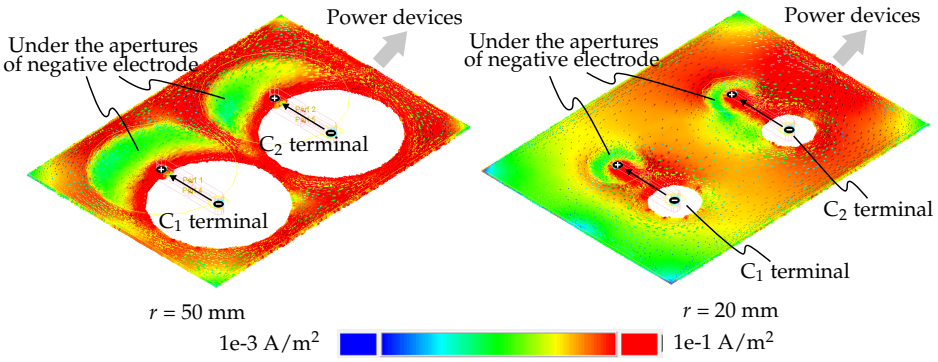


FIGURE 3.7: Current density distribution on the inner surface of the positive electrode at 100 kHz.

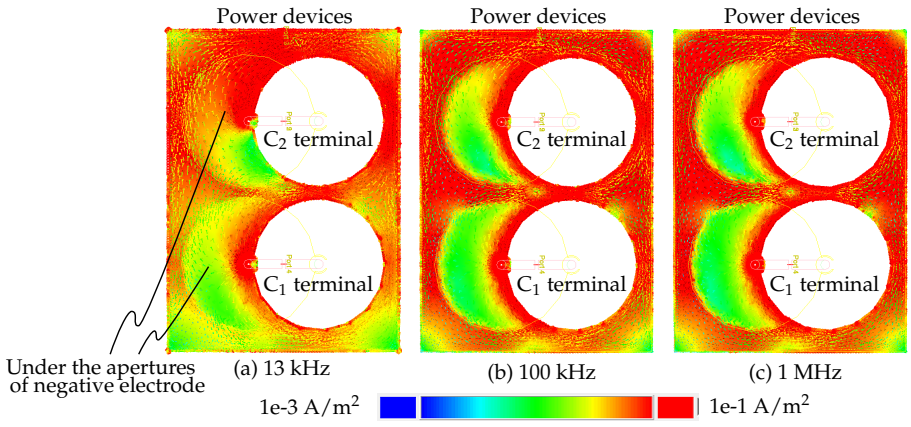


FIGURE 3.8: Current density distribution on the inner surface of the positive electrode with an aperture size of 50 mm.

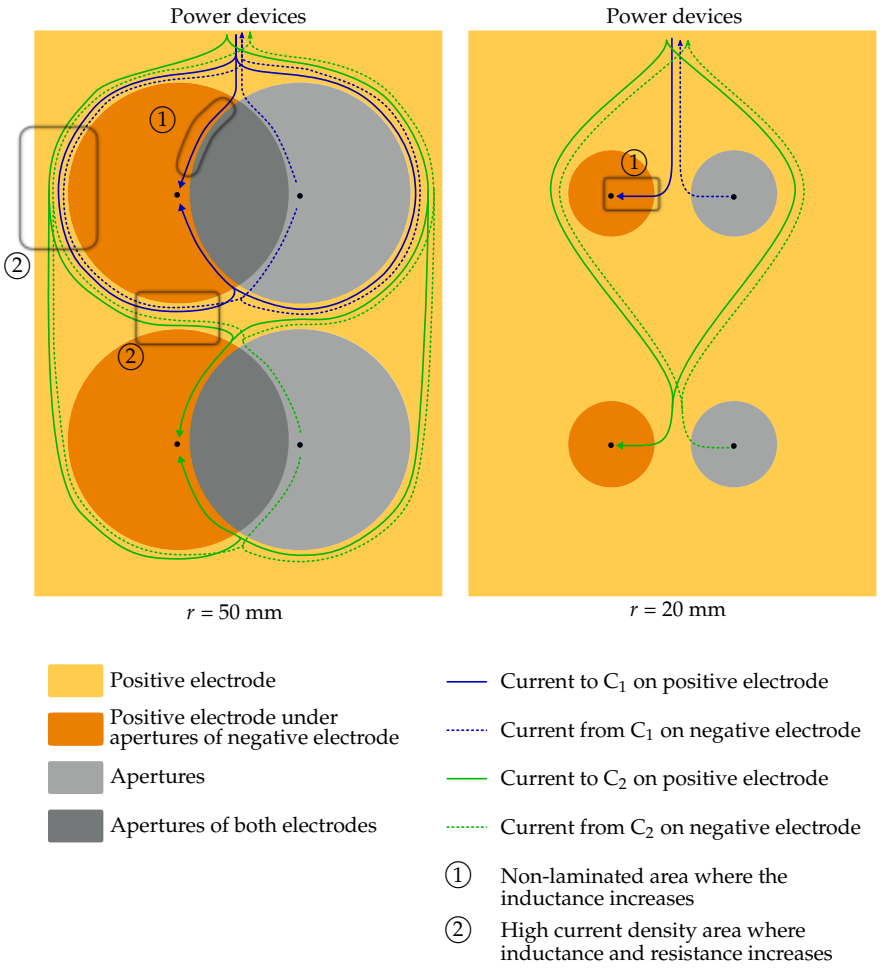


FIGURE 3.9: Explanation of the current distribution on the laminated busbar with apertures.

Fig. 3.7 shows the current density distribution obtained by EM simulation. In general, current mainly flows through the path of lowest impedance, which is the shortest current loop. Thus, the current in the case of $r = 20$ mm focuses to flow in the conductors of the laminated area highlighted in red. On the other hand, the current does not flow much through the conductors under the apertures of the opposite-side electrodes [99]. For example, in Fig. 3.7, there is a conductor on the green area of the positive electrodes, but no conductor exists in the same area on the negative electrode because of the apertures. If the current flows through that non-laminated area on the positive electrode, there is no current on the negative electrode to cancel the flux generated by the current on the positive electrode, thereby increasing parasitic inductance.

Fig. 3.8 shows the current density distribution at different frequencies of 13 kHz, 100 kHz, and 1 MHz. It is evident that the current flows in the non-laminated area

at 13 kHz, that is, there is less green area. Because the impedance of the inductance is low at low frequencies, the current can flow through the non-laminated area. Besides, the current at 100 kHz and 1 MHz concentrates on the laminated area highlighted in red.

Fig. 3.9 shows the detailed diagram of the current distribution.The conductor in the figure is the positive electrode and there are apertures on the negative electrode on the stripe pattern. The gray area is the apertures on the positive electrode. This figure deals with the current that flows from power devices to the capacitors on the positive electrode and from capacitors to power devices on the negative electrode. Blue and green lines show the currents that flow in capacitor C_2 and C_1, respectively.

Regarding the understanding of EM simulation results, the current avoids flowing through the non-laminated area. This current is depicted as arrows in Fig. 3.9. Furthermore, there are two cases that increase the parasitic inductance and resistance.One is the current path on the non-laminated area, highlighted as ①. The larger the aperture size, the longer the path of current on the non-laminated area. In this case, the inductance becomes large because the current on ① is unable to get the effect of mutual inductance.

The second case is the current concentration along the apertures, highlighted as ②. In the conventional understandings of busbars and at low frequencies, there exists much area where the current flows on the positive electrode even though there are apertures on electrodes on the other side. However, EM simulation shows that the current avoids flowing on the non-laminated area at high frequency. At a radius of 50 mm, the current flowing to C_2 especially goes in the detour path because of the apertures for C_1. Therefore, it can be concluded that analysis of parasitic inductance and resistance must be performed considering the apertures on both electrodes at high frequency.

3.2 Analysis of current imbalance between the DC link capacitors

3.2.1 Theoretical analysis

This section shows the principle of current imbalance between two DC link capacitors. Current imbalance occurs because of the impedance imbalance between the current paths. This analysis is based on Fig. 3.4.

From the simplified circuit in Fig. 3.4, the following equations hold:

$$L_1\frac{\mathrm{d}i_{C1}}{\mathrm{d}t} + R_1 i_{C1} + \frac{1}{C_1}\int i_{C1}\mathrm{d}t = L_2\frac{\mathrm{d}i_{C2}}{\mathrm{d}t} + R_2 i_{C2} + \frac{1}{C_2}\int i_{C2}\mathrm{d}t \tag{3.7}$$

$$i_{C1} + i_{C2} = i_{sw} \tag{3.8}$$

where

$$L_x = L_{Cx} + L_{busx} \tag{3.9}$$

$$R_x = R_{Cx} + R_{busx} \tag{3.10}$$

$$C_x = C_{Cx} \tag{3.11}$$

$$x \in \{1, 2\}$$

The solution for eq. (3.7) is as follows:

$$i_{C1} = K_{*1}e^{-\alpha t}\cos(\omega_d t + \theta_*) + K_{*2}t + K_{*3} \tag{3.12}$$

$$i_{C2} = -K_{*1}e^{-\alpha t}\cos(\omega_d t + \theta_*) + K_{*2}t - K_{*3} \tag{3.13}$$

(Case: $*$ = a, c)

$$\begin{cases} K_{*1} = \frac{CD}{\cos(\theta_* + \phi)}\left(\left(\frac{\Delta t}{2} + CR\right)\frac{C_1R_1 - C_2R_2}{C_1 + C_2} - \frac{C_1L_1 - C_2L_2}{C_1 + C_2}\right) \\ K_{*2} = D\frac{C_1}{C_1 + C_2} \\ K_{*3} = -CD\frac{C_1R_1 - C_2R_2}{C_1 + C_2} - \frac{I_{out}}{2}\frac{C_1}{C_1 + C_2} \end{cases} \tag{3.14}$$

(Case: $*$ = b, d)

$$\begin{cases} K_{*1} &= \frac{CD}{\cos(\theta_* + \phi)} \left(\frac{\Delta t}{2} \frac{C_1 R_1 - C_2 R_2}{C_1 + C_2} \right) \\ K_{*2} &= 0 \\ K_{*3} &= \frac{I_{\text{out}}}{2} \frac{C_1}{C_1 + C_2} \end{cases} \tag{3.15}$$

where the asterisk $*$ represents the term among (a) to (d) in eq. (3.5) and Fig. 3.5, θ_* is the initial phase of oscillation, K_{*x} is the coefficient calculated from eqs. (3.14)-(3.15), and ω_{d} is resonant angular frequency. The resonant angular frequency ω_{d} (and resonant frequency f_{d}) is expressed as follows:

$$\omega_{\text{d}} = 2\pi f_{\text{d}} = \sqrt{\frac{1}{(L_1 + L_2) * (\frac{C_1 C_2}{C_1 + C_2})} - \left(\frac{R_1 + R_2}{2(L_1 + L_2)} \right)^2} \tag{3.16}$$

The first term with K_{*1} in (3.12) has an exponential to the power of negative time and a cosine function, which converges to zero. Besides, before the first term converges to zero, the current imbalance occurs because of the parasitics difference such as R_1, R_2, L_1, and L_2. The second term with K_{*2} represents the switching current of slope D depending only on the capacitance of DC link capacitors. If the capacitors are identical, there is no current imbalance in this term. The third term with K_{*3} is a constant coefficient that depends on the capacitance of DC link capacitors and parasitics difference between R_1 and R_2.

Assuming $C_1 = C_2$, the terms in (3.15) has no effect on the current imbalance except for K_{*1}. In terms of (b) and (d), the constant value of K_{*3} is balanced between C_1 and C_2, while the coefficient of damped oscillation, K_{*1}, has an imbalance term depending on R_1 and R_2. This means the rms value of each current is equal if the term of K_{*1} in (3.13) converges to zero. In terms of (a) and (c), K_{*1} has a subtraction term depending on L_1 and L_2. This difference between L_1 and L_2 also causes current imbalance.

3.2.2 Numerical analysis

TABLE 3.1: Constant parameters for the numerical analysis.

	$r = 20$ mm	$r = 50$ mm
I_{out}	20 A	
f_{sw}	20 kHz - 1 MHz	
Δt	20 ns	
C_1, C_2	50 μF	
L_{C1}, L_{C2}	3.55 nH @10 MHz	

*Parasitic parameters of the busbar have frequency characteristics which are the EM simulation results.

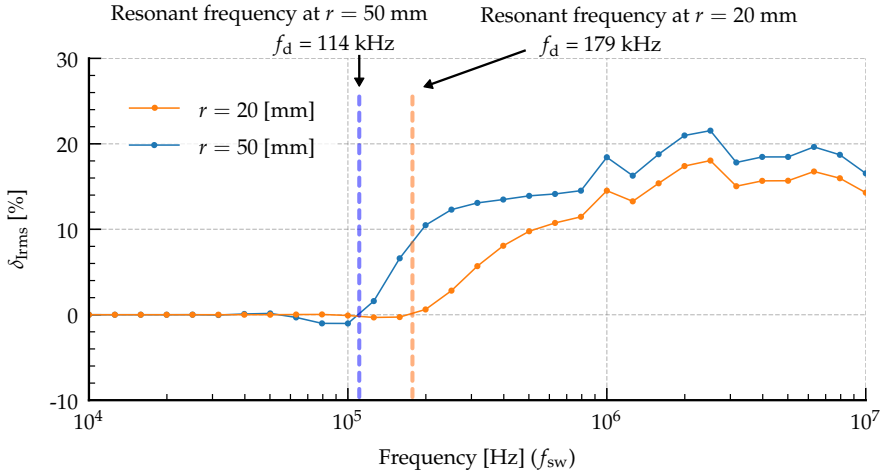
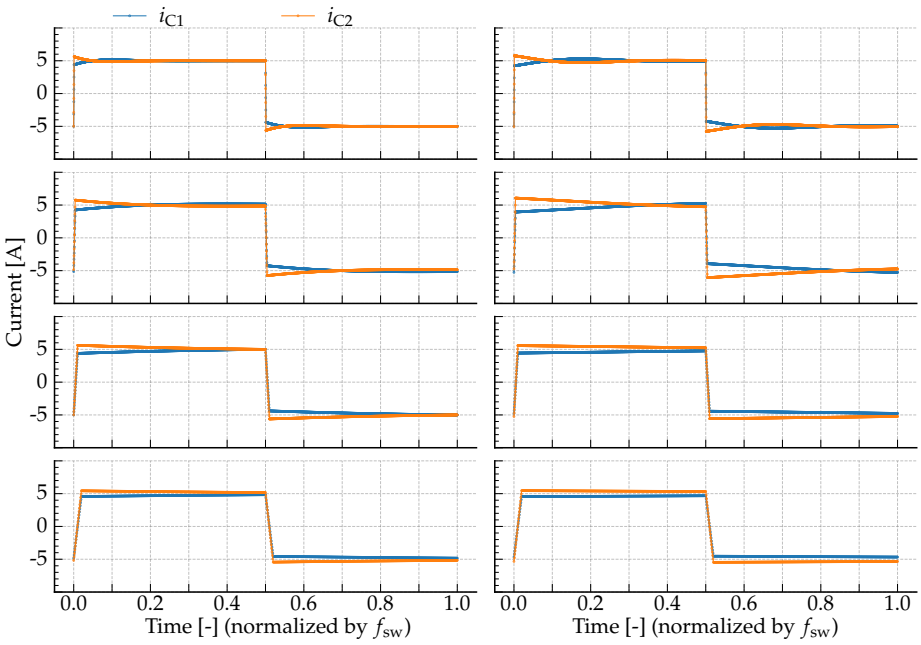


FIGURE 3.10: Current imbalance ratio ΔI_{rms} versus switching frequency f_{sw} with aperture r of 20 and 50 mm.



(a) Clearance $r = 20$ mm (b) Clearance $r = 50$ mm

FIGURE 3.11: Switching waveforms with aperture r = 20 and 50 mm at switching frequency f_{sw} of 50, 200, 500, 1000 kHz.

Based on (3.12)-(3.13), numerical analysis is performed. Table 3.1 shows the constant parameters used in the numerical analysis. For the other parameters such as parasitics of the busbar, the value at the switching frequency is extracted from EM simulation results and used in the numerical analysis. The current imbalance ratio ΔI_{rms} is defined as follows:

$$\Delta I_{rms} = \frac{I_{C2,rms} - I_{C1,rms}}{I_{C1,rms}} \tag{3.17}$$

where $I_{C1,rms}$ and $I_{C2,rms}$ are the rms value of the current i_{C1} and i_{C2}, respectively. Fig. 3.10 shows the relationship between current imbalance ratio ΔI_{rms} and switching frequency f_{sw}. At frequencies, less than 100 kHz, the current imbalance ratio ΔI_{rms} is approximately zero. In the case of $r = 50$ mm, the current imbalance ratio ΔI_{rms} dramatically increases around the resonant frequency of 114 kHz. The waveforms around the resonant frequency can be oberved in Fig. 3.10(b) at 200 kHz. Above the resonant frequency, the current imbalance ratio ΔI_{rms} increases by 20%, where the resonance phenomenon is not seen for this narrow pulse. In the case of $r = 20$ mm, the current imbalance ratio ΔI_{rms} has the same trend as the case of $r = 50$ mm. Because the resonant frequency at $r = 20$ mm is 1.57 times higher than that of at

$r = 50$ mm, the current balances till f_{sw} of 200 kHz. However, above the resonant frequency, current imbalance occurs and leads to the faster degradation of C_2.

Fig. 3.11 depicts the switching waveforms of the current i_{C1} and i_{C2} at frequencies of 50, 200, 500, and 1000 kHz from top to bottom. At 50 kHz, the current oscillation converges to $\frac{I_{out}}{2}$ as expected from the theoretical analysis; At 200 kHz, the switching frequency f_{sw} is similar to the resoant frequency f_d and oscillates above/below $\frac{I_{out}}{2}$. The current, thus, balances even though the oscillation occurs.

3.3 Experimentation

The experimentation is performed along with the following phases: (i) Current sensing method consideration, (ii) experimental environment setup, (iii) implementation of circuit, and (iv) experimental results.

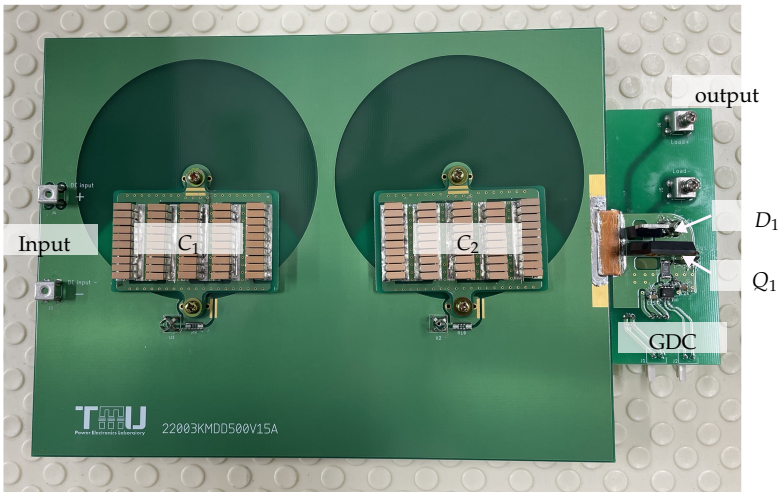


FIGURE 3.12: Photo of the Circuit and busbar.

3.3.1 Current sensing method

In recent technologies, it is still challenging to sense high frequency and high current derivative to time. This study proposes the shunt-resistor-sensing current compensation method considering the frequency characteristics of the shunt resistor. Many papers have discussed the current sensing method by shunt resistors for mainly two cases. One is for the current control in power converters. Another is for experimental visualization, which does not require sensing time; this study focuses on the mentioned case. Hauke et al. [100] have attempted measuring the high $\mathrm{d}i/\mathrm{d}t$ current

with extremely low inductance without disturbing the actual current waveforms. To measure the current, the constant parasitics are considered for calculation. Besides, this study focuses on the frequency characteristics of the shunt resistor because the shunt resistor has frequency characteristics of parasitics at a wide range of frequencies. This method is based on the convolution of a current waveform and a step response of the shunt resistor.

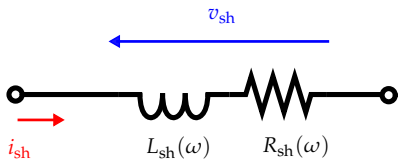


FIGURE 3.13: Equivalent circuits of the shunt resistor.

Fig. 3.13 shows the equivalent circuit of the shunt resistor as an example. The current i_{sh} at low frequencies is calculated from the measured voltage v_{sh} over R_{sh}. For high-frequency current, the voltage v_{sh} is affected by the parasitic inductance L_{sh}, and hence, the current must be compensated by the additional calculation of v_{sh}. One method calculates the product of the Fourier transform of v_{sh} and the inverse of the shunt impedance, then takes the inverse Fourier transform of the result to obtain the current in the time domain. However, this method is suitable for periodical sinusoidal waveforms and not for rectangular and trapezoidal waveforms stimulated by active power devices. This study utilizes the compensation method as given below:

$$\begin{aligned} i_{sh} &= \left(v_{sh} * i_{sh,impulse}\right)(t) \\ &= \int_{-\infty}^{\infty} v_{sh}(\tau) i_{sh,impulse}(t-\tau) d\tau \end{aligned} \tag{3.18}$$

where $i_{sh,impulse}(t)$ is the current impulse response of the shunt resistor. ADS implicitly calculates this impulse response $i_{sh,impulse}(t)$ for convolution.

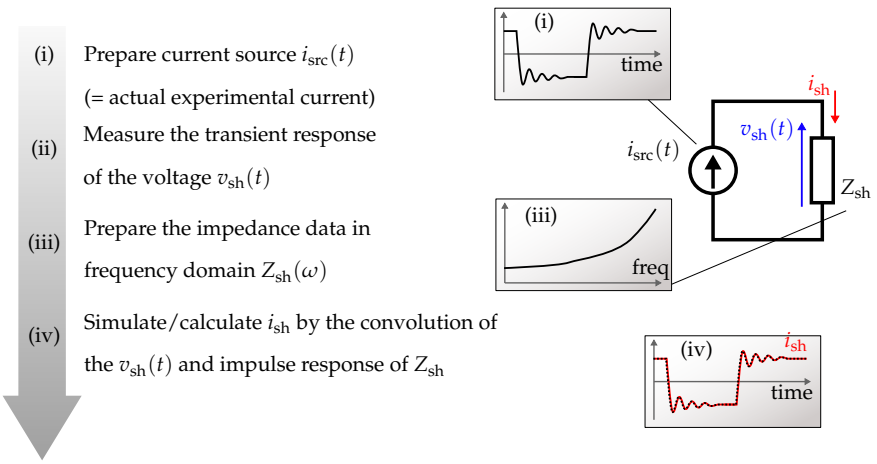


FIGURE 3.14: Current compensation process.

Fig. 3.14 shows the current compensation process. In this study, the ideal current of $i_{src}(t)$ cannot be directly measured, but the voltage of the shunt $v_{sh}(t)$ can be measured instead. In addition, since the frequency characteristics of the shunt resistor is measured by an impedance analyzer, the current $i_{sh}(t)$ is obtained. It should be noted that the obtained current i_{sh} is filtered by a low pass filter to eliminate the high-frequency components above several tens of mega Hertz since the current must have a high-frequency component [97]. The cut-off frequency of the first order low pass filter is 10 MHz. This is effective enough because this study focuses on the circulating current between the capacitors on the DC side at frequencies ranging from a few kHz to 1 MHz.

3.3.2 Double pulse test

A double pulse test (DPT) was performed to validate the analysis and simulation of the current imbalance. The circuit diagram is based on Fig. 3.2. Each component and each piece of equipment are listed in Table 3.2.

TABLE 3.2: Components and equipment for experimentation.

Letter	Description	Product number	Maker	Basic data
Q1	SiC MOSFET	SCT2280KE	Rohm	1.2 kV, 35 A(pulse)
D1	SiC Diode	SCS208KG	Rohm	1.2 kV, 87 A(pulse)
C1, C2	MLCC	FA10	TDK	700 V, 5 μF x 10
-	Oscilloscope	MDA8000	Lecroy	2.5 GS/s, 1 GHz
-	Passive probe	P6139B	Lecroy	500 MHz

Fig. 3.15(a) shows the measured current waveforms at periods of 50 kHz, 200 kHz, 500 kHz, and 1 MHz. It must be noted here that the currents i_{C1} and i_{C2} are measured in a different sessions; the waveforms are superimposed just to see the appearance of current imbalance. It can be seen that the peak current is approximately twice of I_{out} immediately after the switching because of the reverse recovery current in Q1 and D1. Fig. 3.15(b) shows the calculated waveforms for comparison. Theoretical calculation results do not consider these peaks to simplify the discussion because the duration of the peak current is much less than the switching periods where the current imbalance mainly occurs.

At 50 kHz, the current oscillates with the opposite phase in i_{C1} and i_{C2}; the current then dampens toward the value of a half of I_{out}. At 200 kHz, the current oscillates and does not dampen enough to be converged; however, the rms value of the current becomes similar resulting in the no imbalance $\Delta I_{rms} = 0$. At 500 kHz, the current imbalance can be seen. At 1 MHz, the current imbalance occurs, but is not observed in sine curve oscillation. The current imbalance ratio is 21.9%, which is similar to the calculated results. For such high-frequency oscillation, it is difficult to view the oscillation of the sinusoidal curve because the switching period is ten times smaller than the oscillation period.

Fig. 3.16 shows the measured current imbalance ratio ΔI_{rms} with different switching frequencies f_{sw}. In the range of low frequencies ($\leq$ 100 kHz) the maximum current imbalance ratio is 5.1%. Around the resonant frequency, the current imbalance ratio increases to 20.7%, as shown in the calculation results. The maximum value of ΔI_{rms} is 35.9% at 666 kHz, which is twice higher than the theoretical analysis result. These phenomena are confirmed as well as calculated and are avoided during the converter design. The whole tendency of the current imbalance ratio in the experiment agrees with theoretical analysis. The difference between the experimentation and calculation is still large (e.g., a maximum of 10%) with respect to the current imbalance ratio. This absolute value of the difference must be improved in the future work. With respect to the resonant frequency f_r, the difference is 75%, which is acceptable after adding the design margin (the margin is often twice the design objective).

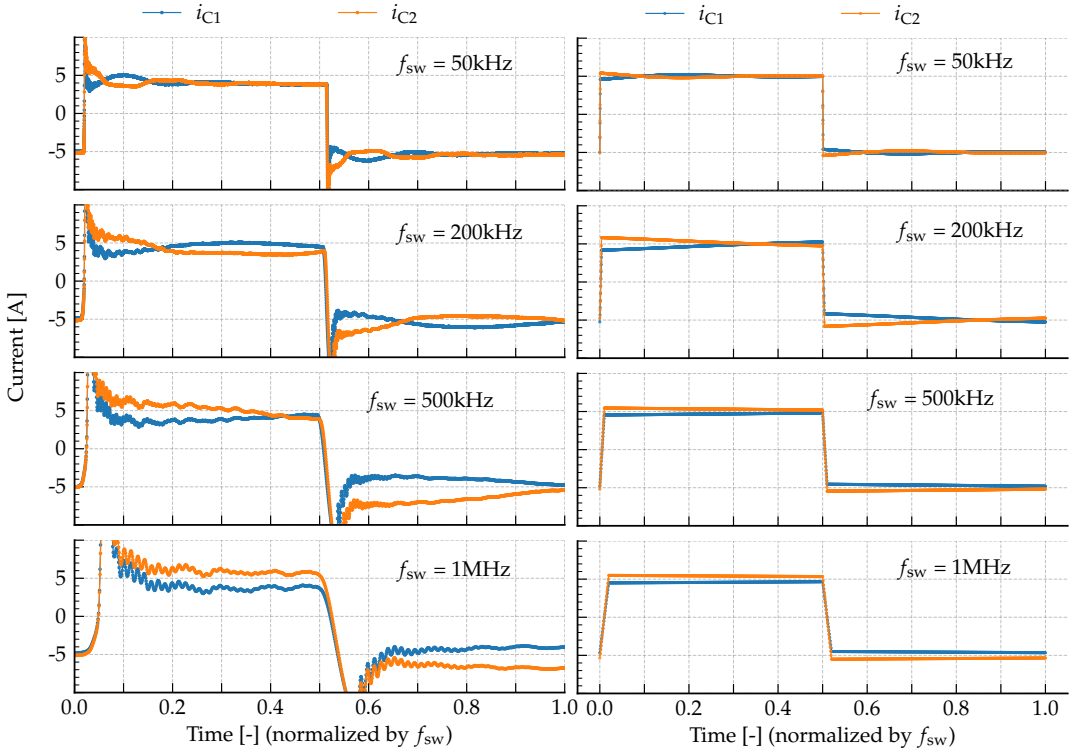


FIGURE 3.15: Experimental waveforms of DPT with aperture size r of 50 mm.

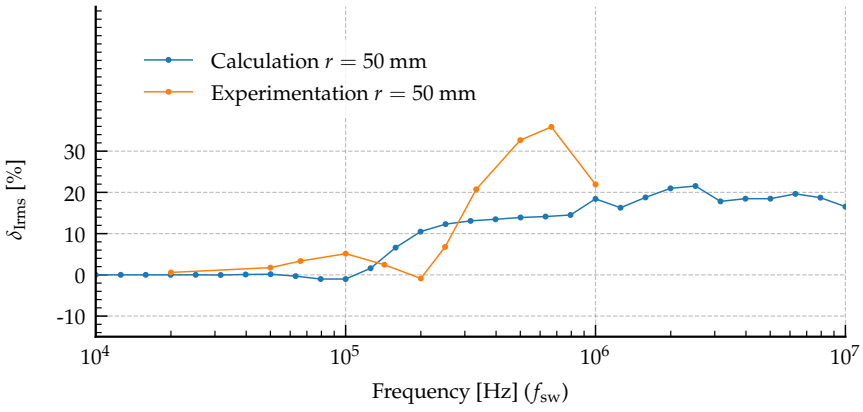


FIGURE 3.16: Experimental results of current imbalance ratio versus switching frequency with aperture size r of 50 mm.

3.4 Conclusion

This study proposed the analysis of the parasitic parameters and current imbalance concering the apertures of the laminated busbar. The increase in parasitic parameters has been confirmed as two main facts from EM simulation, one is the increase in inductance due to the non-laminated area and another is the current concentration.

The difference between inductance and resistance increases by 392% and 302%, respectively, as the aperture size increases. The proposed analysis reveals the current imbalance phenomena among the DC-link capacitors for high-frequency operation of power conversion circuits. In the experimentation section, this study demonstrates the current compensation method for the shunt resistor using convolution analysis.

From the discussions in this study, the authors have concluded the design guideline as follows:

1. The busbars and capacitors can be designed considering the switching frequency and current imbalance ratio with the resonant frequency in the current path among the DC-link capacitors.
   (a) If $f_{sw} \leq f_d$, the current imbalance ratio converges to zero.
   (b) If $f_{sw} \approx f_d$, the current imbalance ratio dramatically increases and unexpected oscillation occurs.
   (c) If $f_{sw} \geq f_d$, the current imbalance ratio converges to a certain value depending on the parasitic parameters.
2. At high switching frequency, the size of the apertures is required to be designed by considering apertures on both electrodes to avoid the large difference of parasitic parameters.

The experimentation validates the proposed procedure using buck converter circuits, rated at 500 V and 20 A. When the switching frequency is around the resonant frequency, a large oscillation is confirmed in experimentation, which is not modeled in the theoretical analysis. To avoid this phenomenon, this study proposed to analyze the resonant frequency considering the parasitic parameters with apertures and avoid using the busbars and capacitors at the switching frequency around the resonant frequency.

Chapter 4

Laminated Busbar Design to Mitigate Parasitic Oscillation

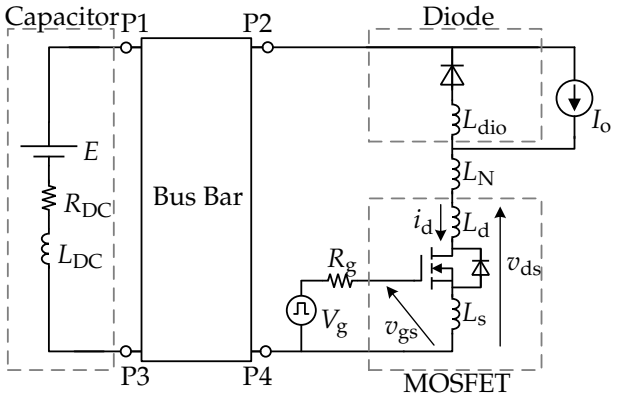
This chapter summerizes the laminated busbar design to mitigate the damped oscillation after power devices switching. Damped oscillation waveforms of current and voltage measured during high-speed switching are a cause of EMI and are difficult to counteract when the natural frequency is in MHz or higher. In addition to the EMI problem, it is also known to be a factor responsible for malfunctioning of power conversion circuits. In particular, when the power circuit wiring and control signal wiring are coupled by magnetic and electric fields, damped oscillation waveforms propagate and affect the operation of the control circuit. Since the damped oscillations are caused by parasitic components in the capacitors and power devices on the DC side, including busbars, it is necessary to design parasitic parameters aggressively to suppress the oscillations.

During the analysis of parasitic parameters, in many cases, the damped oscillation waveform equation is approximated and analyzed with a single frequency and damping factor combination. However, the effect of parasitic components becomes more pronounced owing to miniaturization, which results in the formation of multiple current loops and the complex behavior of the damped oscillation waveforms, making it impossible to apply conventional analysis methods as they are. In the literature, the resonant frequency due to the parasitic component is derived analytically by taking into account the parasitic capacitance of the busbar, but the damping coefficient cannot be calculated because the parasitic resistance is ignored. Since this

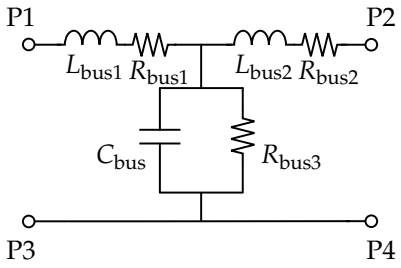
parasitic resistance oscillates at natural frequencies above several MHz, the resistance of the conductor increases due to skin effect and proximity effect. However, since the AC resistance varies with the conductor geometry and frequency, it is difficult to simulate it in the circuit analysis stage. Fig. 4.1 shows the buck chopper circuit discussed in this dissertation. The laminated busbar is expressed as a 2-port network for general expression. In this analysis, T-type equivalent circuit is adopted to consider the capacitance and conductance.

In the literature, it has been shown that the AC resistance of busbars has a significant effect on damped oscillations. The author has performed an analysis considering the parasitic inductance and capacitance of the busbars and the AC resistance.

The attenuation analysis discussed in this chapter contributes to reducing electromagnetic noise, which is a problem when applying high-speed switching, simplifying filters, and analyzing noise propagation inside circuits in detail.



(a) Buck chopper circuit.



(b) T-type equivalent circuit of bus bar.

FIGURE 4.1: Circuit configuration.

4.1 Frequency characteristics of parasitic resistance and conductance of laminated busbars

4.1.1 Electromagnetic simulation to extract parasitic parameters

Parasitic parameters are extracted by electromagnetic field analysis using the finite element method for the laminated busbar shown in Figure 4.1, which is the DC side wiring of the buck chopper circuit. Figure 4.2 shows the structure of a laminated busbar, in which currents flow in opposite directions to each other in the positive and negative conductors that sandwich the insulator. Since the cross-sectional area A of the conductor is expressed as the product of the conductor thickness t and width w, the DC resistance is equal when the cross-sectional area is constant. On the other hand, since the AC component flowing through the busbar during switching reflects the AC resistance considering the skin effect and proximity effect, the resistance value increases as the frequency increases.

The software used for the analysis is the finite element method of ADS (Keysight Technology). The governing equations are obtained by Maxwell's equations as given below:

$$\nabla \times \left(\frac{1}{\dot{\mu_r}} \cdot \nabla \times \boldsymbol{E} \right) - k_0^2 \dot{\varepsilon_r} \boldsymbol{E} = 0 \tag{4.1}$$

where $\dot{\varepsilon_r}$ is complex relative permittivity, $\dot{\mu_r}$ is complex relative permeability, and $k_0 = \omega\sqrt{\mu_0 \varepsilon_0}$. The electric field $\boldsymbol{E}$ is a three dimensional space vector. The conductor material is Cu (conductivity $\sigma = 5.8 \times 10^7$ S/m) and the insulator material is FR4 (relative permittivity $\epsilon_r = 4.6$, dielectric tangent tanD $= 0.016$ (1 GHz) from datasheet). The relative permittivity model is described in detail later. In Figure 4.2, the terminals are installed at the positive and negative electrodes of the busbar conductor. To assume the experimental terminal condition, the lead wires are connected to the terminals in their lower direction, and electric field as the excitation field is applied between the wires in the opposite side of the terminals. Figure 4.3 depicts the simulation space to be calculated. Here, let the excitation fields be E_{ext1} and E_{ext2}. Based on the electric field excited, the electromagnetic fields in the model space is calculated. The absorption boundary condition is applied to the boundary

of the model space. The model space size ℓ_{hight} and ℓ_{width} are 2 m and the busbar is located in the center of the model space. The power of reflection and transmission is, then, calculated at the terminals of the excitation field. The electromagnetic model is equivalently expressed as a circuit schematic as shown in the right of Fig. 4.3. The voltage sources V_{ext1} and V_{ext2} correspond to the excitation fields E_{ext1} and E_{ext2}, respectively. The simulated electromagnetic fields are treated as a black box that is equivalently a 2-port network circuit. S-parameters are then calculated based on the power of reflection and transmission, so that the Z-parameters are achieved.

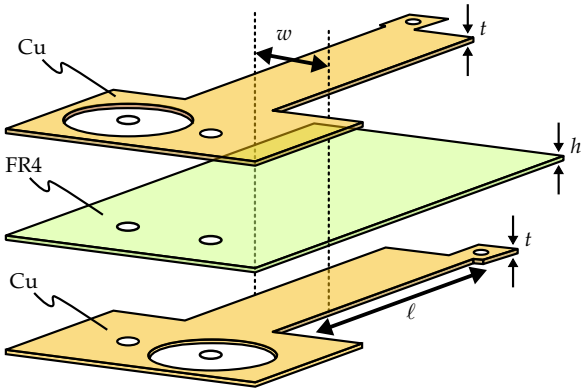


FIGURE 4.2: Busbar Structure.

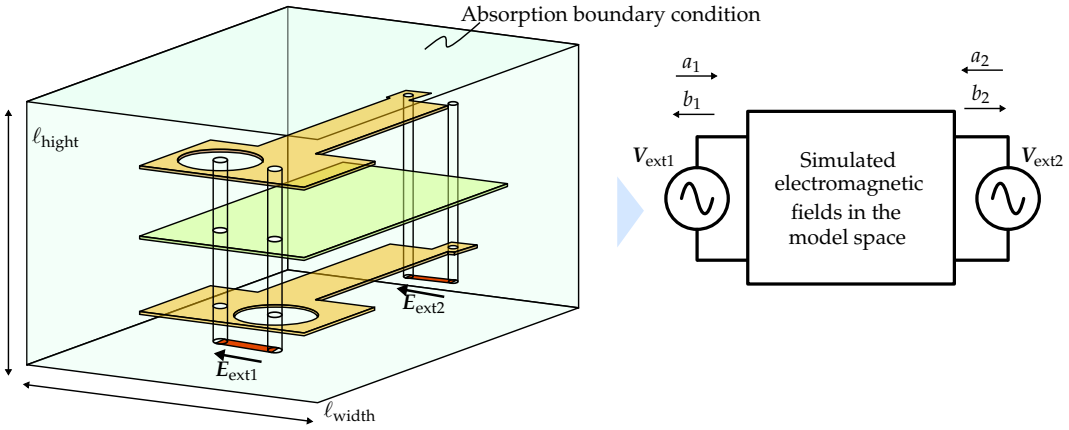


FIGURE 4.3: A model space and exitation field for electromagnetic simulation.

The busbar is represented as a 2-terminal pair network with the P1 terminal as positive and the P3 terminal as negative and the P2 terminal as positive and the P4 terminal as negative to obtain $S_{11}, S_{12}, S_{21}, S_{22}$. The mesh is automatically generated by the Adaptive Mesh function of ADS, which generates a coarse mesh at all frequencies to be analyzed and calculates the S-parameters. Next, the number of

meshes is increased and the S-parameters are calculated again to obtain the rate of change of the S-parameters. The mesh was increased by a factor of 1.25. The mesh subdivision is repeated until the rate of change of the S-parameter is less than 0.01 at all frequencies to be analyzed, and the mesh is used for the analysis within the frequency range to be analyzed. Note that the absorption boundary condition was used as the boundary condition.

Table 4.1 shows the physical parameters of the three busbar structures. Taking these busbar structures as examples, the author analyzes the frequency response of the parasitic parameters. Figure 4.4 shows the analytical results of the frequency response of the parasitic parameters for the three types of busbars.

It is observed that the smaller the insulation thickness and the larger the conductor width, the smaller the inductance and the larger the capacitance.

TABLE 4.1: Bus bar structure of three models.

Model	t	h	w	ℓ
①	0.8 mm	5.2 mm	5.0 mm	90 mm
②	0.105 mm	1.6 mm	38 mm	90 mm
③	0.035 mm	0.4 mm	114 mm	90 mm

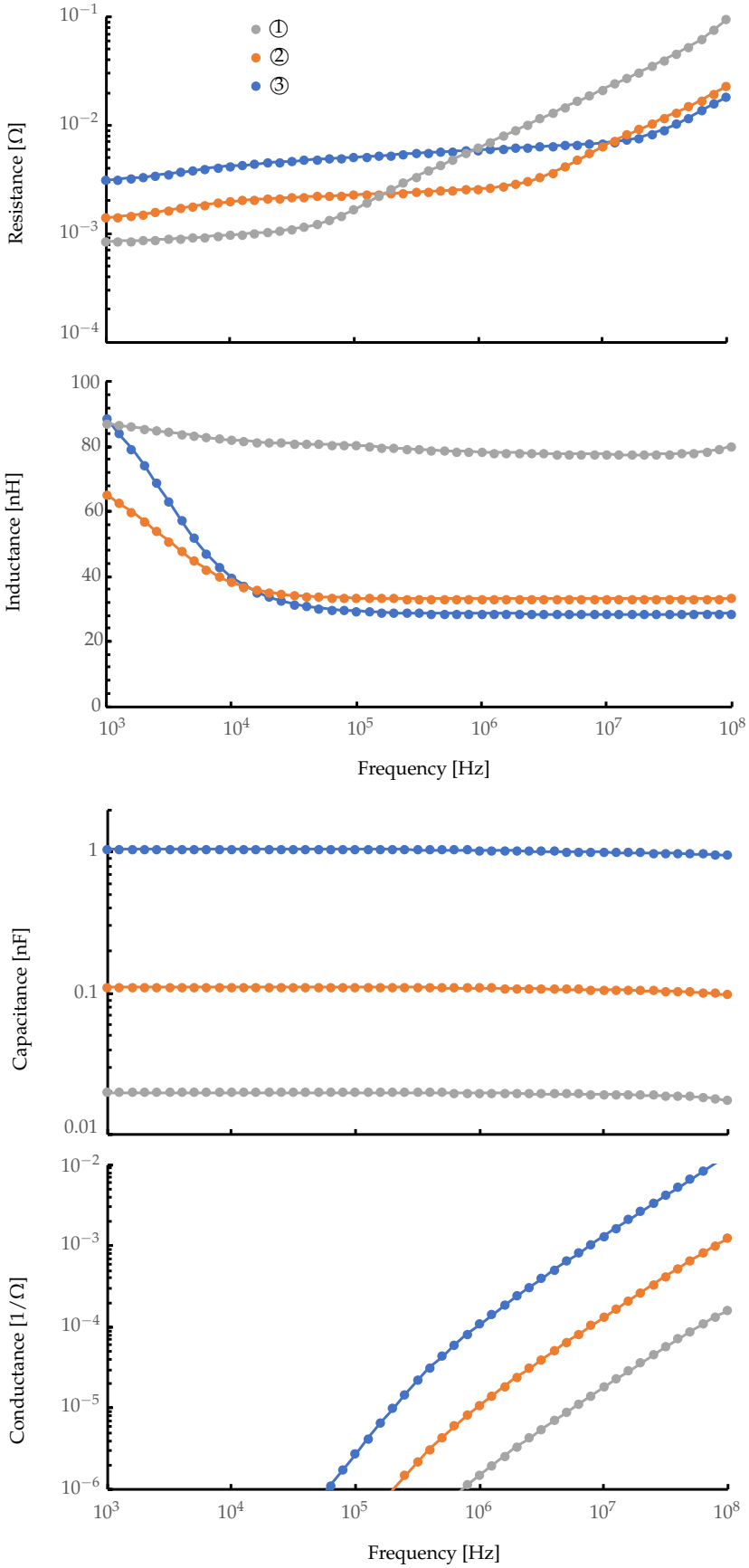


FIGURE 4.4: Parasitic parameters of busbar ①−③.

Figure 4.5 shows the simulated and measured AC resistance of Busbar III. The agreement between the measured and simulated results indicates the validity of the resistance map. Note that only the region below 30 MHz is shown in this chapter because the measurement accuracy cannot be sufficiently ensured for high-frequency components.

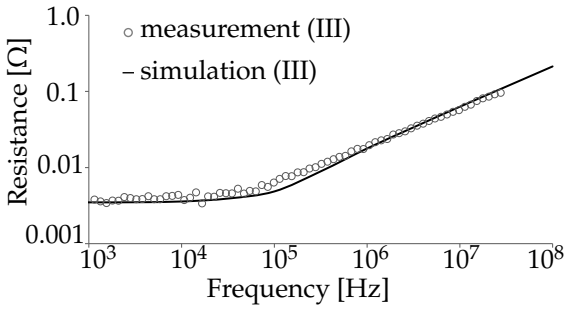


FIGURE 4.5: Frequency characteristics of laminated-busbar resistance.

4.1.2 Correction of dissipation factor

Even though the AC resistance of the busbar was simulated in the previous section, the trend was consistent, but the absolute values were very different. Next, the dielectric loss, which is the loss part related to attenuation, is modeled together with the measured values. The busbar resistance R_3 represented by the T-type equivalent circuit that is derived from the dielectric loss. The R_3 is represented by the equation (4.2) using the dielectric tangent tanD.

$$R_3 = \frac{1}{\omega C_{\mathrm{bus}} \mathrm{tanD}} \tag{4.2}$$

where ω is the angular frequency. Since the value in the datasheet is 0.016 (1 GHz), R_3 can be calculated using C_{bus} obtained from the simulation.

Figure 4.6 is the busbar used to measure R_3. This busbar was connected to the impedance analyzer E4990A (Keysight technology) and R_3 was measured.

Figure 4.7 shows the adjusted values of the dielectric tangent tanD of the busbar parasitic capacitance C_{bus} and the values from the datasheet. It is confirmed that the two intersect at a frequency of approximately 10^6 Hz. Since the natural frequency of the damped oscillation waveform that occurs immediately after switching is several

MHz to hundreds of MHz, the resistance R_3 is small in this frequency region, which greatly affects the damping characteristics.

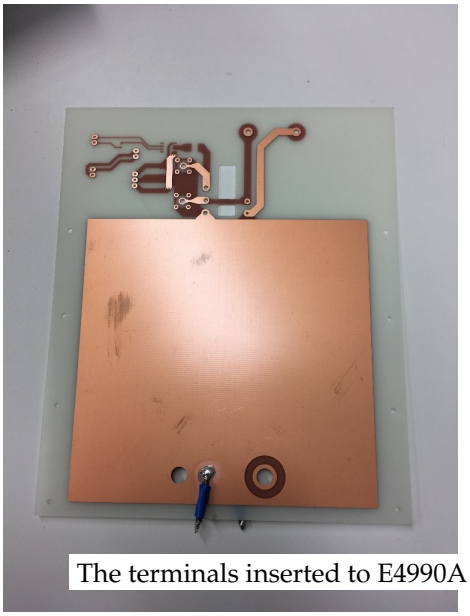


FIGURE 4.6: The bus bar to measure the tanD.

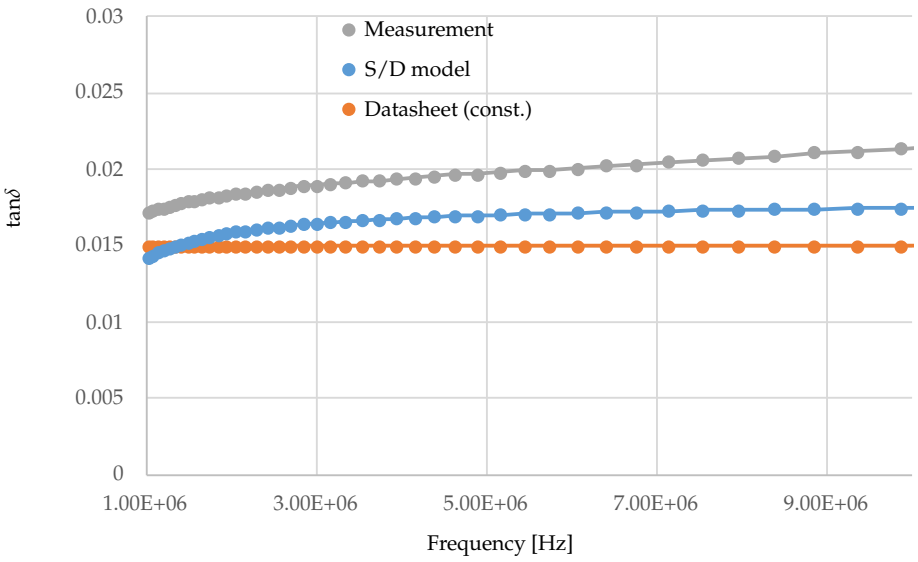


FIGURE 4.7: Comparison of tanD adjusted and datasheet.

The EM software, ADS, is able to utilize the dielectric loss model with frequency charactristics. ADS deals with Svensson/Djordjevic model [94], [101] as follows:

$$\dot{\varepsilon_r}(freq) = \varepsilon_1 + a \cdot \frac{f_H + j \cdot freq}{f_L + j \cdot freq} \tag{4.3}$$

where $\dot{\varepsilon_r}(freq)$ is complex relative permittivity, ε_1 is a part of a real part of complex relative permittivity, a is a coeffiecient, and f_H and f_L are the upper and lower limits of the frequency. To transform this equation to tanD, the following equation holds:

$$\tan D = \frac{a \cdot \arctan\left(\frac{freq(f_H - f_L)}{f_H f_L + freq^2}\right)}{\varepsilon_1 + \frac{1}{2}a \cdot \ln\left(\frac{freq^2 + f_H^2}{freq^2 + f_L^2}\right)} \tag{4.4}$$

This model preserve causality not to violate physical phenomena [94]. The tangent delta increases at a certain frequency and decreases at the higher frequency. In this dissertation, the parameters are set as the following condition:

TABLE 4.2: Svensson/Djordjevic Model parameters.

ε_1	4.6
a	0.06
f_H	1 THz
f_L	300 kHz
f_{tanD}	2 MHz
tanD	0.019

The dielectric constant of electric field dependent is not considered since the dielectric constant of the dielectric material FR-4 does not have the electric field dependency, which means the linear dielectric with constant permittivity with respect to the applied electric field [102], [103].

4.2 Coupled oscillation analysis

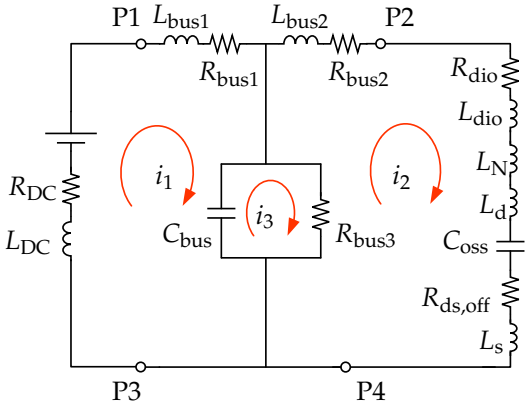


FIGURE 4.8: Equivalent circuit of buck chopper when MOSFET turns off.

In the frequency domain, the amplitude of the frequency spectrum at the natural frequencies increases as $\mathrm{d}i/\mathrm{d}t$ increases. Let f_r denote this natural frequency. Since the damped oscillation waveform oscillating at the natural frequency is a source of electromagnetic noise, let V_ds be the magnitude at f_r of the discrete Fourier transform of this V_r. The magnitude of V_r is used to evaluate the electromagnetic noise.

Figure 4.8 is the equivalent circuit of Figure 4.1. The current loop $i_1 \sim i_3$ is defined as in Figure 4.8.

First, the following equation holds

$$
\begin{aligned}
&\begin{bmatrix} L_1 & 0 & 0 \\ 0 & L_2 & 0 \\ 0 & 0 & 0 \end{bmatrix}
\begin{bmatrix} \frac{\mathrm{d}^2 i_1}{\mathrm{d}t^2} \\ \frac{\mathrm{d}^2 i_2}{\mathrm{d}t^2} \\ \frac{\mathrm{d}^2 i_3}{\mathrm{d}t^2} \end{bmatrix} \\
&+ \begin{bmatrix} R_1 & 0 & 0 \\ 0 & R_2 + R_{\mathrm{bus3}} & -R_{\mathrm{bus3}} \\ 0 & -R_{\mathrm{bus3}} & R_{\mathrm{bus3}} \end{bmatrix}
\begin{bmatrix} \frac{\mathrm{d}i_1}{\mathrm{d}t} \\ \frac{\mathrm{d}i_2}{\mathrm{d}t} \\ \frac{\mathrm{d}i_3}{\mathrm{d}t} \end{bmatrix} \\
&+ \begin{bmatrix} \frac{1}{C_{\mathrm{bus}}} & 0 & -\frac{1}{C_{\mathrm{bus}}} \\ 0 & \frac{1}{C_{\mathrm{oss}}} & 0 \\ -\frac{1}{C_{\mathrm{bus}}} & 0 & \frac{1}{C_{\mathrm{bus}}} \end{bmatrix}
\begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \mathrm{O}
\end{aligned}
\tag{4.5}
$$

$$L_1 = L_{\mathrm{DC}} + L_{\mathrm{bus1}} \tag{4.6}$$

$$R_1 = R_{\mathrm{DC}} + R_{\mathrm{bus1}} \tag{4.7}$$

$$L_2 = L_{\mathrm{bus2}} + L_{\mathrm{dio}} + L_{\mathrm{N}} + L_{\mathrm{d}} + L_{\mathrm{s}} \tag{4.8}$$

$$R_2 = R_{\mathrm{bus2}} + R_{\mathrm{dio}} + R_{\mathrm{ds,off}} \tag{4.9}$$

where $\mathbb{O}$ is a zero matrix. In this section, the current loop $i_1 \sim i_3$ is obtained by numerical analysis. The general solution for i_1 is expressed as

$$\begin{aligned} i_1 = {} & A_{11}\, e^{-\zeta_1\omega_1 t} \sin(\omega_1 t) + A_{12}\, e^{-\zeta_2\omega_2 t} \sin(\omega_2 t) \\ & + A_{13}\, e^{-\zeta_3\omega_3 t} \sin(\omega_3 t) \end{aligned} \tag{4.10}$$

$$\omega_{\mathrm{x}} = 2\pi f_{\mathrm{x}} \qquad (\mathrm{x} = 1 \text{ to } 3) \tag{4.11}$$

where, $A_{11} \sim A_{13}$ is the initial amplitude, $\zeta_1 \sim \zeta_3$ is the damping factor, $\omega_1 \sim \omega_3$ is the eigenangular frequency, $f_1 \sim f_3$ are eigenfrequencies. The currents I_2 and I_3 have the same general solution as I_1. The combination of attenuation coefficients and natural frequencies depends on the parasitic parameters of the circuit. For example, when two eigenfrequencies exist, there is a damping factor corresponding to the eigenfrequency. The natural frequencies and damping factors are calculated by solving equation (4.5).

TABLE 4.3: Parameters of Fig. 4.8 for analysis and calculated result.

d_1	78 mm	6 mm
L_1	90 nH	47 nH
L_2	25.5 nH	24.2 nH
C_{bus}	1160 pF	1160 pF
C_{oss}	27 pF	27 pF
R_{DC}	68 mΩ	55 mΩ
$R_{\text{dio}} + R_{\text{ds,off}}$	850 mΩ	794 mΩ
R_{bus1}	49 mΩ	17 mΩ
R_{bus2}	49 mΩ	57 mΩ
R_{bus3}	552 Ω	552 Ω
f_1	15.4 MHz	21.3 MHz
f_2	194 MHz	199 MHz
ζ_1	0.015	0.011
ζ_2	0.014	0.014
$\zeta_1\omega_1$	2.31×10^5	2.34×10^5
$\zeta_2\omega_2$	2.72×10^6	2.79×10^6

To check the validity of the calculation method, the experimentation is performed. The experimentation utilizes two cases; the distance between the capacitance terminals d_1 is 78 mm and 6mm. When the distance is long such as 78 mm, the parasitic inductance of the capacitor and busbar increase and the resonant frequency must be lower than that in the case of 6 mm. Table 4.3 shows the circuit constants and calculation results for d_1 = 78 mm and 6 mm. At d_1 = 78 mm, the damping factor ζ_1 has a value similar to ζ_2, while the natural frequency f_1 is 12.5 times smaller than that of f_2. This is because of the larger product of ζ_2 and f_2, which can be attenuated faster than the combination of ζ_1 and f_1.

Comparing the terminal-to-terminal distance d_1 = 78 mm and 6 mm, the difference in $\zeta_1\omega_1$ is less than 1%, but there is more error in the natural frequencies. However, because the parasitic inductance at d_1 = 6 mm is 50% smaller than at d_1 = 78 mm, the surge voltage is likewise smaller and therefore the initial amplitude is also smaller.

4.2.1 Simulation results

Circuit simulations were performed while varying D_1. Table 4.3 lists the parasitic parameter. The input voltage is 500 V and the output current is 30 A.

Figure 4.9 is one cycle of the drain-source voltage v_{ds}. The switching waveform at d_1 = 6 mm during device turn-off is observed to decay faster than at d_1 = 78 mm.

Figure 4.10 is the discrete Fourier transformed frequency spectrum of v_{ds}. In the frequency domain, the peak value V_r at the eigenfrequencies d_1 = 6 mm is smaller than at d_1 = 78 mm.

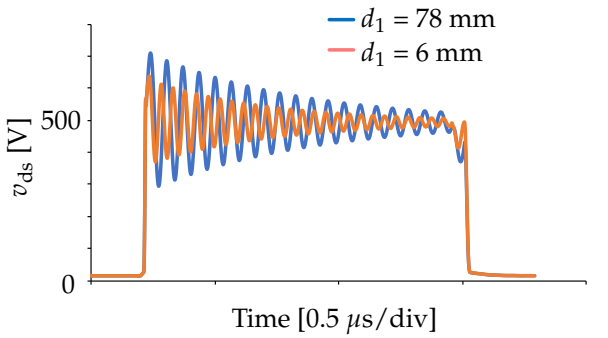


FIGURE 4.9: Simulated switching waveforms of v_{ds} at d_1 = 6 mm and 78 mm.

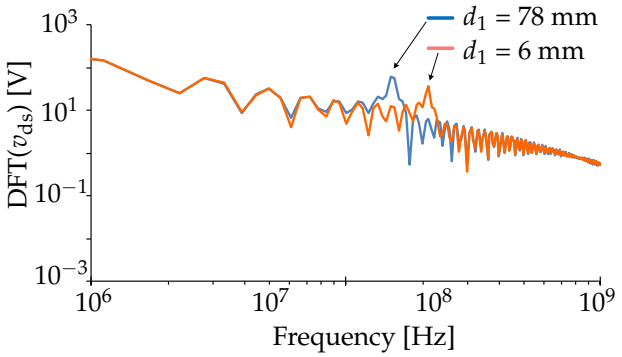


FIGURE 4.10: Simulated DFT of v_{ds} at d_1 = 6 mm and 78 mm.

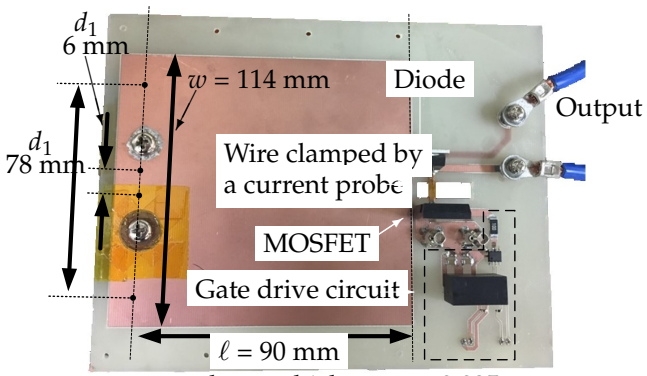
4.2.2 Experimental results

Figure 4.11 shows the experimental circuit. The power devices used are SiC MOSFET (SCT2280KE, Rohm) and SiC diode (SCS205KG, Rohm). The parasitic inductance of the power devices is measured by the TDR method, and is equal to 8 nH and 7 nH

for the MOSFET and diode, respectively. The input voltage and output current are 500 V and 30 A, respectively.

Figure 4.12 shows the experimental waveform. As in the simulation waveform, the amplitude of the damped oscillation waveform becomes smaller when d_1 = 6 mm. Figure 4.13 is the discrete Fourier transform of the drain-source voltage v_{ds}. The peak value for d_1 = 6 mm is 48% smaller than that for d_1 = 78 mm.

Table 4.4 compares the simulated and experimental results. It is observed that changing d_1 from 78 mm to 6 mm lowers the peak value of the frequency spectrum V_r by 47% for both simulation and experiment. The relative error of the eigenfrequencies is less than 3.3%, which is a good agreement between the simulation and experimental trends.



conductor thickness t = 0.035 mm
insulator height h = 0.4 mm

FIGURE 4.11: Detail of the experimental circuit.

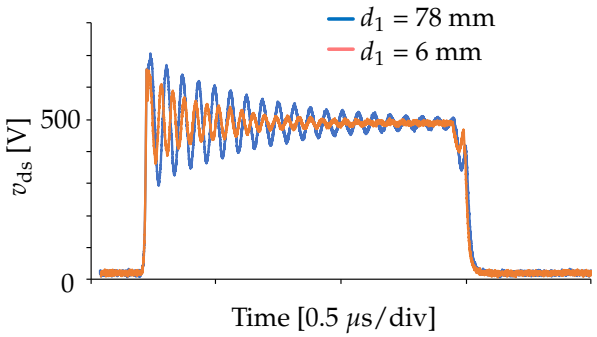


FIGURE 4.12: Experimental switching waveforms of v_{ds} at d_1 = 6 mm and 78 mm.

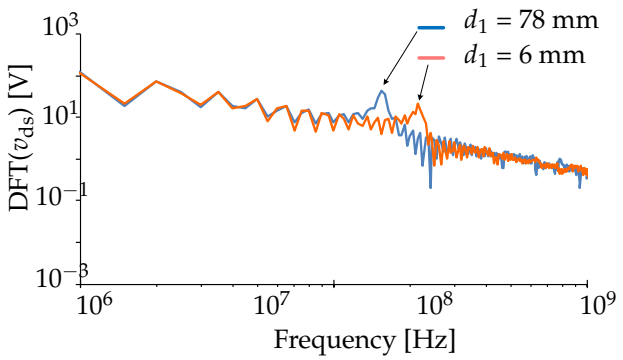


FIGURE 4.13: Experimental DFT of v_{ds} at d_1 = 6 mm and 78 mm.

TABLE 4.4: Comparison of simulation and experimentation.

Simulation		
	d_1 = 6 mm	d_1 = 78 mm
Resonant frequency	21.1 MHz	15.0MHz
Damping factor	0.017	0.017
Peak value V_r in frequency domain	37 V	71 V
Experimentation		
	d_1 = 6 mm	d_1 = 78 mm
Resonant frequency	21.5 MHz	15.5 MHz
Damping factor	0.029	0.025
Peak value V_r in frequency domain	22 V	42 V

4.3 Design of damping characteristics to mitigate the oscillation based on the laminated busbar relevant map

Using the parasitic parameter maps, including the AC resistance and dielectric loss, the relationship between the busbar structure and the natural frequency and damping coefficient is clarified. A plot visualizing this relationship enables the design of busbar structures to obtain arbitrary damping characteristics.

4.3.1 Target circuit

The natural frequencies and damping coefficients in the range of the parasitic parameter map of the busbar were analyzed for the circuit in Fig. 4.1 and the equivalent circuit in Fig. 4.8. Parameters other than the busbar were assumed to be constant values. Table 4.5 are the circuit constants used in the analysis.

TABLE 4.5: Parameters of Fig. 4.1 for Damping factor map.

L_{DC}	freq. dependent
$L_{dio} + L_N + L_d + L_s$	24.2 nH
C_{oss}	40 pF
R_{DC}	freq. dependent
R_{dio}	127 mΩ
$R_{ds,off}$	freq. dependent

The frequency dependent parameters are measured by using an impedance analyzer. In the out of measured frequency range, the parameters are extrapolated as a constant value. $R_{ds,off}$ is also known as a voltage dependent parameter, thus, the measured value at highest voltage bias in the impedance analyzer (40 V) was applied.

4.3.2 Damping coefficient map

Because of the frequency characteristics of the busbar parasitic parameter map, the busbar parasitic parameters applied to the equivalent circuit in Figure 4.8 must be the values at the natural frequency. For example, if a coupled oscillation analysis of equation (4.5) is performed using the parasitic parameter map at a frequency of 1 kHz, the natural frequency will be several MHz. Since the frequencies of the parameters used and the calculated natural frequencies are different, the natural frequency values cannot be trusted and the parasitic parameters at the natural frequencies must be used. Therefore, the author matched the eigenfrequencies with the parasitic parameters used according to Figure 4.14. First, the frequency to be analyzed is determined (I), and a coupled oscillation analysis is performed with the parasitic parameters at that frequency (II). Next, the frequency set in (I) is checked to

see if the calculation results agree with the frequency set in (I) and (III). If they do not match, increase the frequency at which the parasitic parameters are extracted and return to the flow in (I). If they match, multiply the calculated natural frequencies by the attenuation coefficients to obtain the attenuation characteristics.

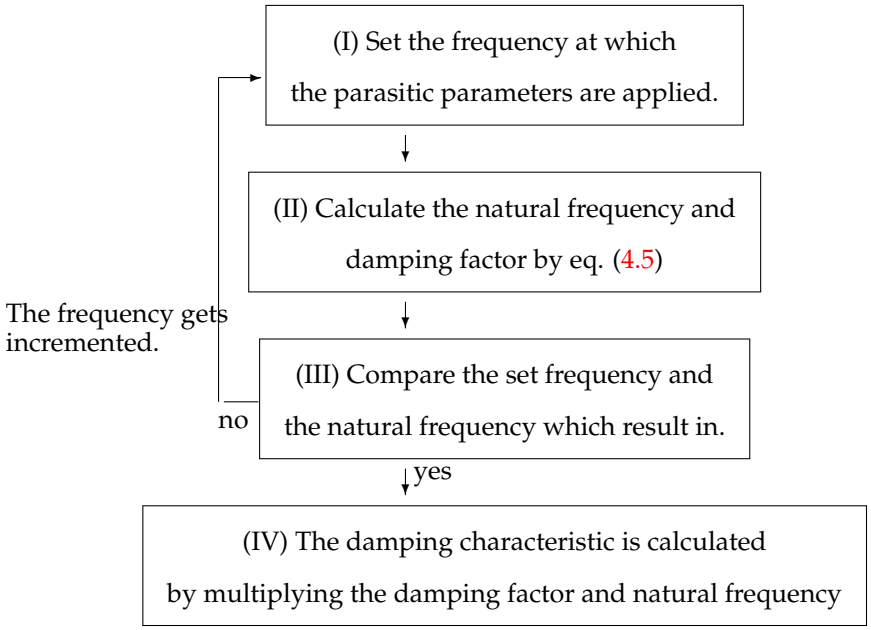


FIGURE 4.14: Procedure of electro-magnetic and circuit simulation by sweeping the geometry of the bus bar.

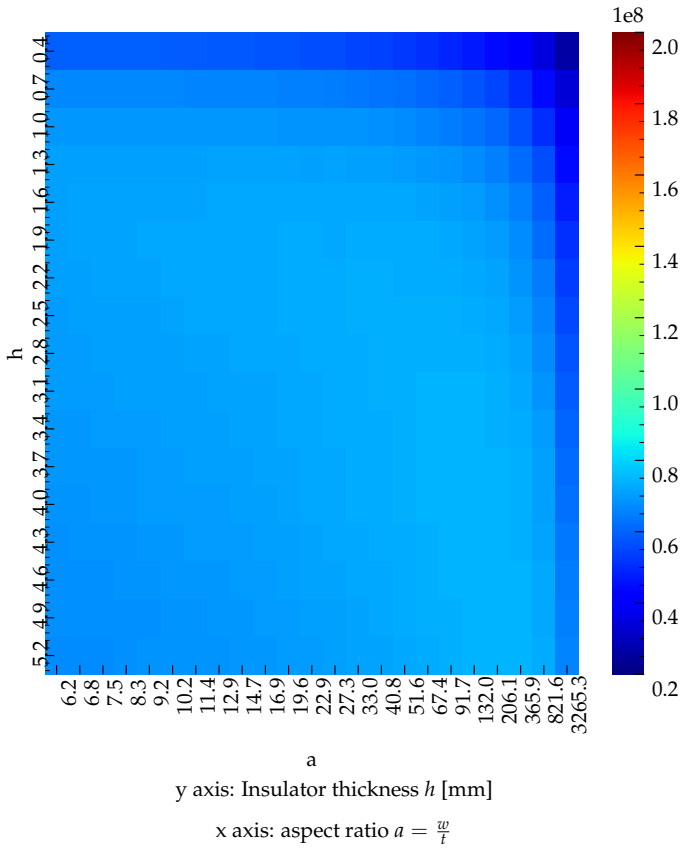
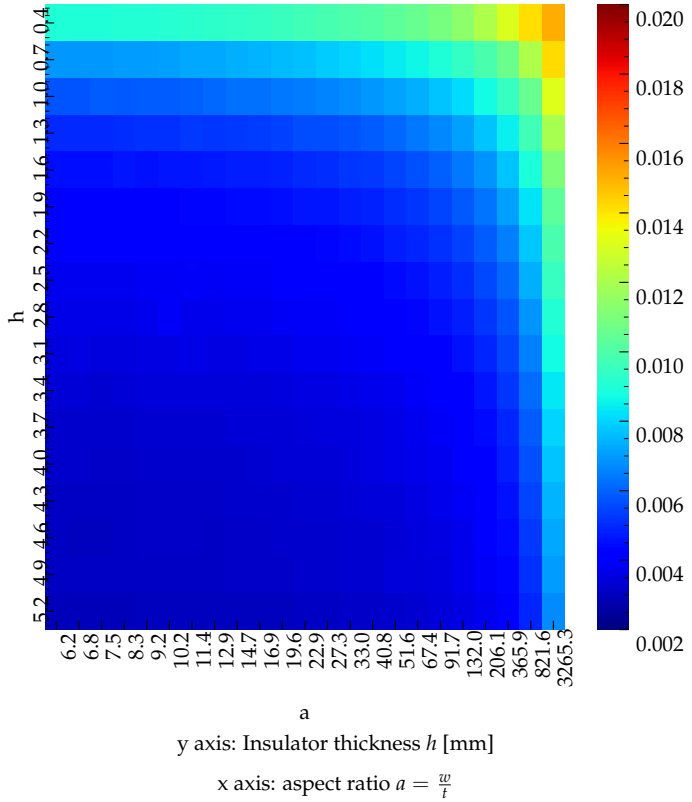


FIGURE 4.15: Frequency map with parasitic conductance.

Figure 4.15 shows the relationship between natural frequency and busbar structure. The natural frequency tends to decrease as the aspect ratio a of the conductor cross section increases and the insulation thickness h decreases. When a = 3265 and h = 0.4 mm, the natural frequency is 27.6 MHz. Thus, the relationship between the natural frequency and the busbar structure varies in a complex manner, indicating that it is necessary to consider the influence of parasitic capacitance, in addition to the higher natural frequency due to skin and proximity effect.



y axis: Insulator thickness h [mm]

x axis: aspect ratio $a = \frac{w}{t}$

FIGURE 4.16: Damping coefficient map with parasitic conductance.

Figure 4.16 shows the relationship between damping coefficient and busbar structure. The tendency of the value is opposite to the natural frequency. As the aspect ratio a increases and h decreases, the damping coefficient increases. Since this analysis includes the parasitic conductance, the higher value is confirmed comparing with the conventional analysis result (shown in the last of this section).

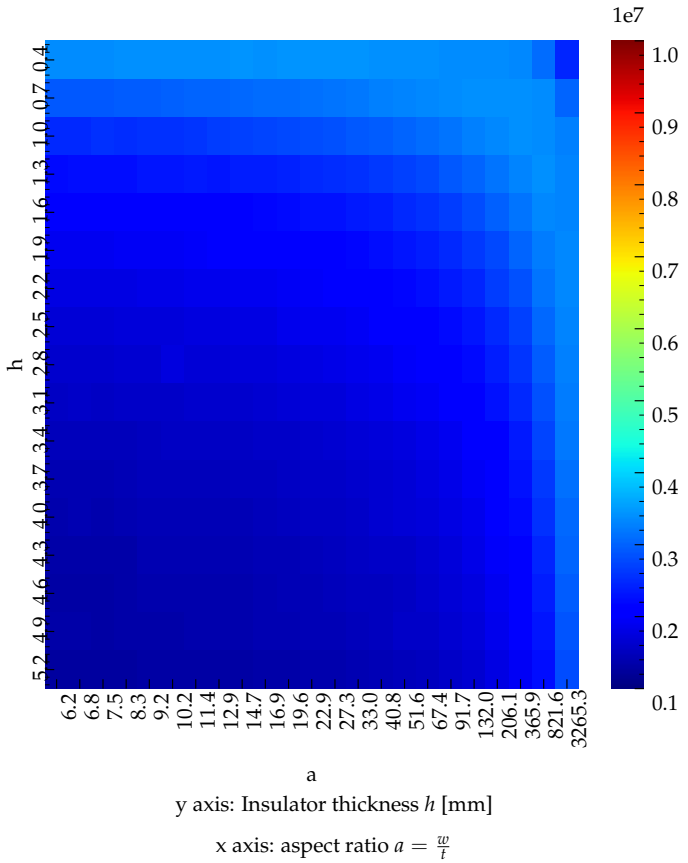
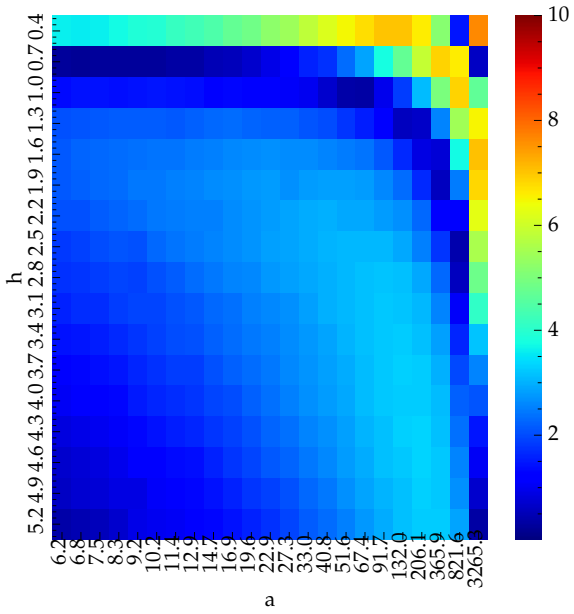


FIGURE 4.17: Damping characteristics map with parasitic conductance.

Figure 4.17 shows the relationship between damping characteristics and busbar structure. The damping characteristics can be calculated by the product of resonant angular frequency and damping coefficient with frequency characteristics such as AC resistance and dielectric loss. The product results in the high damaping characteristics band, from upper left to lower right in the figure. Thus, to mitigate the oscillation, this band will be advantages on the fast decay. To consider the amplitude after the switching to a certain time, the initial amplitude must be calculated.



y axis: Insulator thickness h [mm]

x axis: aspect ratio $a = \frac{w}{t}$

FIGURE 4.18: Amplitude map with parasitic conductance.

Figure 4.18 shows the relationship between amplitudes and busbar structure. The amplitude also has low and high value bands in the figure. This band is based on not only the parasitic parameters but also the switching transient time. As for the frequency of 27.6 MHz (a=3265 and h=0.4), the half period is 18 ns which is approximately the switching transient time. This can be revealed by the numerical and analytical calculations.

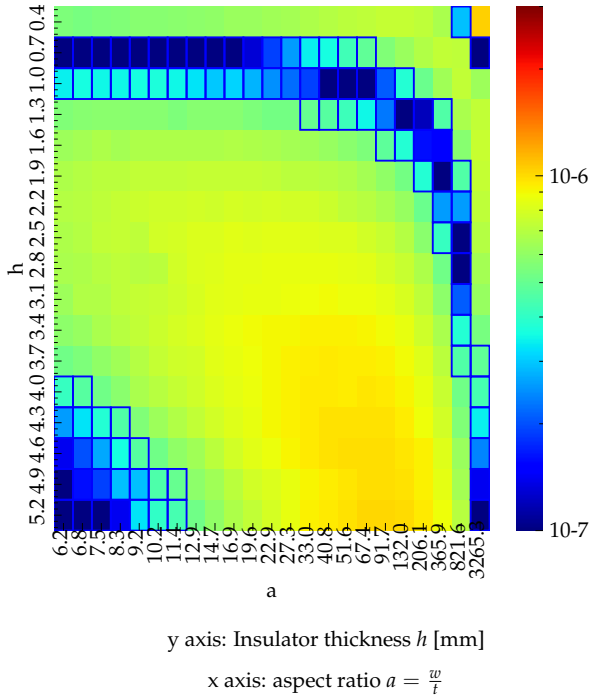
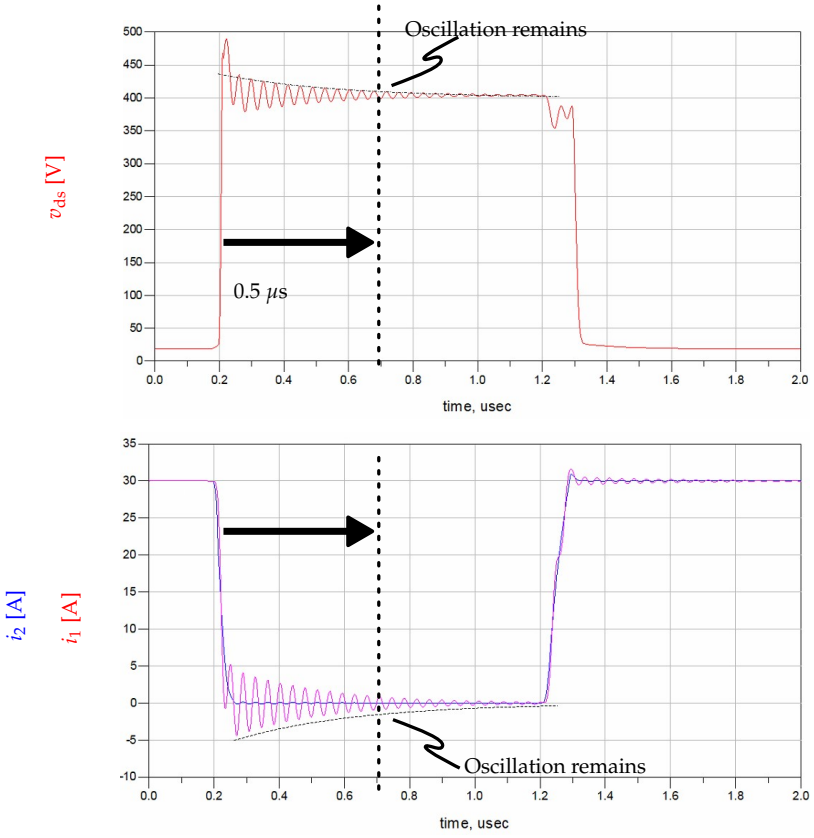


FIGURE 4.19: Design map that indicates decay time to the 2% of output current.

Figure 4.19 shows the relationship between decay time and busbar structure. This decay time map can be achieved from the previously shown maps. In this case, the DC side current oscillates mainly in the loop of DC link capacitor and busbar capacitance. The design objective of amplitude at a certain time is 2% of the output current (0.6 A). The longest decay time is seen in the busbar structure having a=3265 and h=0.4 mm. In addition, from the amplitude and damping characteristics map, there are bands that dampen the oscillation faster. The highlighted area as blue box is the design range that satisfy the design objective (i_1=0.6 A at 0.5 μs after switching. It is evident that the conventional busbar design will fail in this evaluation since the busbar which has the lowest inductance does not satisfy the design objective of the decay time. Using this design map, it is possible to design arbitrary attenuation characteristics and to discuss the attenuation after a certain time of power device switching. Furthermore, since the relationship with the busbar structure is clear, it is also possible to design the busbar structure.



h=0.4 mm and t = 0.035 mm

FIGURE 4.20: Simulation waveforms corresponding to the out of design points in Fig. 4.19.

Figure 4.20 shows the simulatoin waveforms based on the busbar structures shown in Fig. 4.19 when h = 0.4 mm and t = 0.035 mm. It can be confirmed that the switching waveform shows the good agreement with the analysis. The error of the calculated decay time is 26% with respect to the simulation. The difference is acceptable since the design margin is often set to twice of the design objective value. Thus, this analysis has been validated.

4.4 Summary

In chapter 4, the author analyzed damped oscillation waveforms and proposed a busbar structure design method to obtain switching waveforms with arbitrary damping characteristics. Coupled oscillation analysis was performed using an equivalent circuit with parasitic parameters that cannot be expressed by the conventional parasitic oscillation equation. By considering the parasitic parameters of the busbar and

the circuit, the parasitic parameters with frequency characteristics were calculated in terms of values at natural frequencies, and the relationship with the busbar structure was clarified. Also, the parasitic conductance greatly decays the damped oscillation waveforms.

For the design point of view, the time domain design method was validated. Based on the damping characteristic map, the design range is analyzed and visuallized. By choosing the geometry of the laminated busbar in that range, the less oscillation waveform will be achieved even though the high-speed switching is applied.

Chapter 5

Laminated Busbar Design to Mitigate both Surge Voltage and Peak Amplitude at Resonant Frequency

This chapter proposes a design procedure for the switching waveform considering a bus bar geometry. In this proposed procedure, two items—the surge voltage and damped oscillation—are evaluated to achieve user-defined design objectives for realizing the optimized switching waveform. This study targets a bus bar geometry for high-speed switching using wide band-gap devices; thus, parasitic parameters in the power converter are considered. The parasitic parameters, which are the inductance, capacitance, conductance, and AC resistance, of the bus bar are analyzed by finite element analysis (FEA) because it should be discussed the frequency characteristics for realizing the optimum switching waveform. The experimentation is performed using buck converter circuits, rated at 400 V and 30 A.

5.1 Switching waveform and evaluated items

This section defines the evaluated items in the switching characteristics such as the surge voltage, damped oscillation level, and switching loss. Each switching characteristic relates the parasitic parameters shown in chapter II.

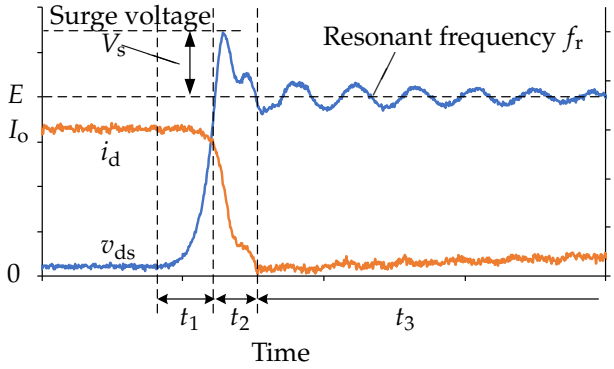


FIGURE 5.1: Typical turn-off waveform of a MOSFET.

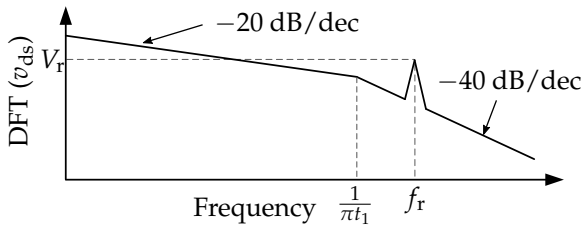


FIGURE 5.2: One example in the spectra envelope of trapezoidal switching waveforms v_{ds}, which has the damped oscillation in one term switching.

Fig. 5.1 shows a typical switching waveform under turn-off operation. The surge voltage V_s is evaluated because it may destroy the power device. This is because of the high di/dt, which induces a voltage between the stray inductance as the electromagnetic force. As mentioned in chapter 2, the maximum drain-source voltage is defined as the surge voltage to be evaluated.

$$V_s = \max(v_{ds}) \tag{5.1}$$

When MOSFET turns off, parasitic inductance, capacitance, and resistance forms a resonant circuit in the converter circuit. The pulse current and voltage made by power devices stimulate the resonant circuit, resulting in the oscillation of the drain current i_d and drain-source voltage v_{ds}. It can be observed that the damped oscillation level becomes high when the parasitic capacitance of the bus bar is too large. The resonant frequency of the damped oscillation is determined as f_r by parasitic parameters, including the bus bar. Then, the derivative of drain current di_d/dt is

one of the components that decides the amplitude of voltage v_{ds} oscillation. In addition, the spectrum at the resonant frequency becomes larger as di/dt is much larger when applying high-speed switching devices. Thus, the gate resistor also affects the damping oscillation because it can control the switching speed. Fig. 5.2 shows an example in the spectra envelope of the switching waveform v_{ds}, which has the damped oscillation after the devices switching. The spectrum is calculated by the discrete Fourier transform (DFT). Assuming that the switching waveform is trapezoidal, the magnitude of the spectrum decreases by 20 dB/dec till $1/\pi t_1$, and then decreases by 40 dB/dec. Besides, the spectrum has a peak value at the frequency f_r if the trapezoidal waveform has the damped oscillation. The peak value has a major effect in terms of electromagnetic interference, and hence, this peak value V_r of the discrete Fourier transform of v_{ds} is taken as one of the parameters to evaluate the switching waveform. This chapter concentrates on the evaluation of the damped oscillation level in the frequency domain and does not focus on the detailed characteristics of the damped oscillation in time domain.

$$V_r = DFT(v_{ds})|_{f=f_r} \tag{5.2}$$

From the discussion above, the surge voltage V_s and damped oscillation V_r will be evaluated.

5.2 Design strategy

5.2.1 Strategy to optimize the switching waveform

This chapter explains the ways optimize the switching waveform. The relationship of the bus bar structure with the parasitic parameters has already been mentioned in section II, and the relationship of the parasitic parameters and switching characteristics in section III. This indicates the switching characteristics are designable by the bus bar structure. The evaluated items such as V_s and V_r cannot be minimized simultaneously. They have different order, then these items have to be normalized

to evaluate them equally so that normalization is applied:

$$V_{\mathrm{sn}} = \frac{V_{\mathrm{s}} - V_{\mathrm{s,min}}}{V_{\mathrm{s,des}} - V_{\mathrm{s,min}}} \tag{5.3}$$

where V_{sn} is the normalized surge voltage V_{s}, $V_{\mathrm{s,min}}$ is the minimum value of V_{s}, and $V_{\mathrm{s,des}}$ is the design value of V_{s}.

$$V_{\mathrm{rn}} = \frac{V_{\mathrm{r}} - V_{\mathrm{r,min}}}{V_{\mathrm{r,des}} - V_{\mathrm{r,min}}} \tag{5.4}$$

where V_{rn} is the normalized peak value of DFT(v_{ds}) V_{r}, $V_{\mathrm{r,min}}$ is the minimum value of V_{r}, and $V_{\mathrm{r,des}}$ is the design value of V_{r}.

TABLE 5.1: Symbols used in (5.3)–(5.4).

Symbol	Description
V_{s}	Surge voltage
$V_{\mathrm{s,min}}$	Minimum value of V_{s}
$V_{\mathrm{s,des}}$	Design value of V_{s}
V_{r}	Peak value of DFT(v_{ds})
$V_{\mathrm{r,min}}$	Minimum value of V_{r}
$V_{\mathrm{r,des}}$	Design value of V_{r}

TABLE 5.2: Swept variables.

	t	h
Minimum value	0.035 mm	0.4 mm
Maximum value	0.8 mm	5.2 mm

Table 5.1 summarizes the symbols in (5.3)–(5.4). The minimal values are obtained by a number of simulation results. These minimal values change if the boundary conditions in Table IV change. Thus, the minimal values are firstly simulated with the boundary conditions. In the design procedure, the minimal values need to be updated if the evaluated items lower than the current minimum values are obtained from the simulation. Circuit designers can determine the design values to satisfy the specification of the power converter circuit. By using these design values in (5.3)–(5.4), the switching waveform is optimized to achieve all design values. If the surge voltage is equal to the minimal value, the normalized surge voltage becomes zero. If the surge voltage is equal to the design objective, the normalized surge voltage

becomes one. Thus, the normalized value takes the value between 0 and 1 if the design variables satisfy the objectives. That is the reason for the minimal value being seen in the numerator and denominator in the normalized equations. The damped oscillation level can be evaluated as well.

The objective function denoted as e_{obj} is defined as

$$e_{\text{obj}} = \sqrt{V_{\text{sn}}^2 + V_{\text{rn}}^2} \tag{5.5}$$

When $e_{\text{obj}} \leq \sqrt{2}$ and all evaluated items are less than 1, which means all design values are satisfied, the pair of the laminated bus bar structure and gate resistor is available. In this chapter, those pairs are defined as the optimal points. The design parameters are the bus bar structure and gate resistor that are swept to find the minimum point of e_{obj}.

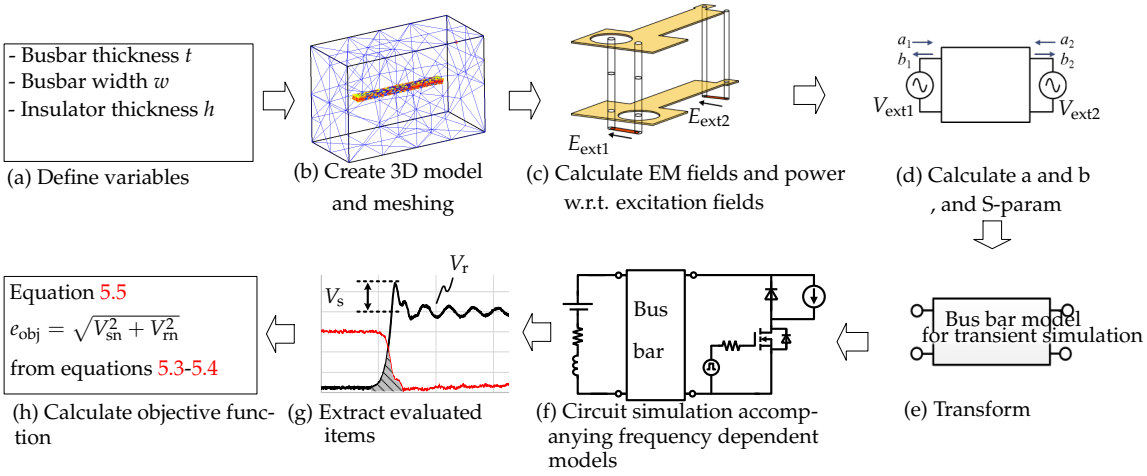


FIGURE 5.3: Design procedure considering the frequency characteristics of laminated busbar parasitics.

5.2.2 Simulation setup

Fig. 5.3 shows the design procedure proposed in this chapter. The simulator ADS is able to handle not only the FEA but the circuit simulation as well. To include the frequency characteristics, the simulator ADS performed the FEA and circuit simulation according to Fig. 5.3. First, the geometric bus bar parameters are defined in Fig. 5.3(a), and then, the bus bar model is generated as a three-dimensional (3-D) geometry model in Fig. 5.3(b). ADS automatically generates and meshes the 3-D bus bar model. From Fig. 5.3(b)-(d), the S-parameters of the bus bar are computed along

with the calculations described in chapter 4. In phase Fig. 5.3(e), the transient and convolution simulation is performed including the S-parameters model of the bus bar, which is able to calculate the transient simulation with the frequency-dependent model such as S-parameters[27]. After the transient and convolution simulation finishes, the data of the waveforms is obtained as the results of the simulation. The results are then evaluated by the surge voltage, damped oscillation, and switching loss in phase Fig. 5.3(f). The surge voltage is obtained from the maximum voltage in the data. To calculate the damped oscillation, discrete Fourier transform is performed with respect to the drain-source voltage v_{ds}. The switching loss is numerically calculated integrating the product of the drain-source voltage v_{ds} and drain current i_{d}. The values of the evaluated items are then numerically calculated by normalization equations according to (5.3)–(5.4), and then, the objective function is calculated by numerical analysis in phase Fig. 5.3(g).

The values in Table 5.2 are known as the boundary conditions since they decide the minimum or maximum values of the evaluated items in the objective function. With respect to t, the minimum thickness of 0.035 mm is selected because it is the standard thin thickness of PCB manufacturers. Moreover, thickness less than 0.035 mm causes the busbar width since the cross-section is set to a constant value of 4 mm. The maximum thickness of 0.8 mm is selected because it is the maximum limit of the PCB manufacturer. The length of the bus bar is set to a constant value of 90 mm. The number of simulations is 715, and the objective function $e_{\mathrm{obj}}$is applied to all waveforms.

TABLE 5.3: Circuit parameters for simulation.

	Symbol	Value
Bus bar length	ℓ	90 mm
Input voltage	E	400 V
Output current	I_{o}	30 A
ESR of the DC link capacitor	R_{DC}	130 mΩ
ESL of the DC link capacitor	L_{DC}	15 nH
Parasitic inductance of the SBD	L_{dio}	7 nH
Parasitic inductance of the MOSFET	$L_{\mathrm{d}} + L_{\mathrm{s}}$	8 nH
Parasitic inductance between the SBD and MOSFET	L_{N}	10 nH

Table 5.3 lists the circuit parameters for simulation. The input voltage E is set to 400 V, and the output current I_o is 30 A. In this simulation setup, $V_{s,des}$ is set to 120 V, which is 30% of the input voltage, and $V_{r,des}$ is set to 1 V, which is 0.4% of the AC component at the fundamental frequency.

5.2.3 Simulation results

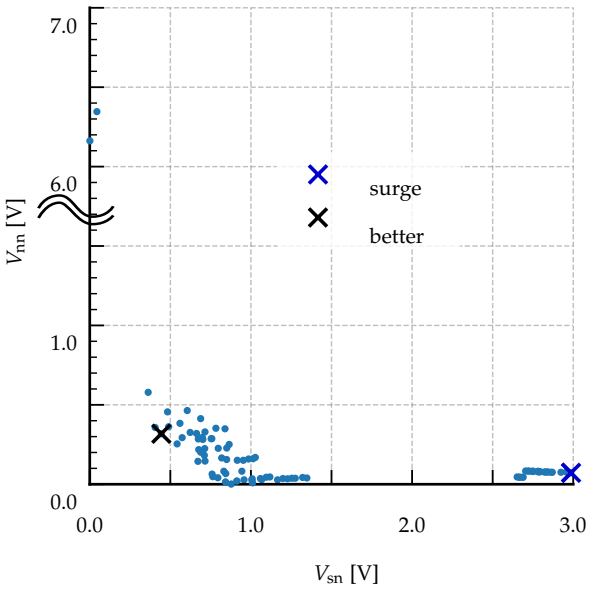
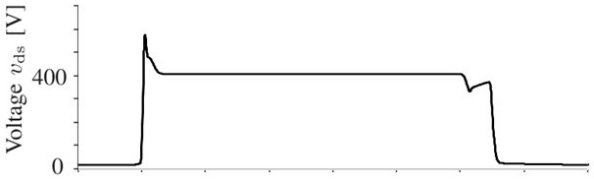


FIGURE 5.4: Design simulation results.

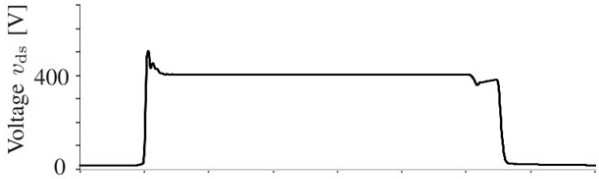
Fig. 5.4 shows the simulated points with respect to the evaluated items of surge voltage and damped oscillation. It can be observed that the surge voltage and damped oscillations are in a trade-off relationship.

If the objective is not satisfied in this configuration, the gate resistor can be increased. However, the switching loss must be carefully designed.

Fig. 5.5 shows the simulation waveforms during MOSFET turn-on and off operations. The waveform that do not satisfy the design objective have a large level of surge voltage as shown in Fig. 5.5 (b). On the other hand, the waveforms that satisfy the design objectives are shown in Fig. 5.5(a). It is evident that the bus bar geometry needs to be designed based on this proposed procedure to achieve the optimal waveform.



(a) Designed busbar (w = 38 mm, t = 0.105 mm, h = 1.6 mm)



(b) Busbar with large surge voltage (w = 5 mm, t = 0.8 mm, h = 5.2 mm)

FIGURE 5.5: Simulation waveforms highlighted in Fig. 5.4.

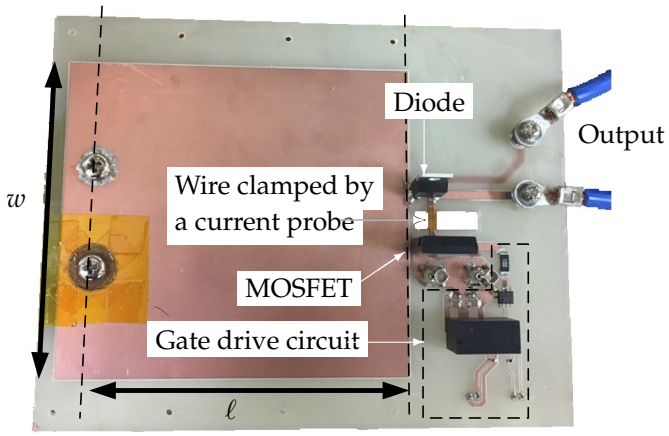


FIGURE 5.6: Details of the experimental circuit.

5.3 Experiments

5.3.1 Experimental setup

Experimental result is presented to confirm the proposed method. Table 5.4 lists the parameters of the power devices used in these circuits. The SiC MOSFET (SCT2280KE, Rohm) and SiC diode (SCS205KG, Rohm) were used in this experiment. Table 5.3 lists the parameters of each component, which are same as the simulation. R_{DC} and L_{DC} are measured by an impedance analyzer at 10 MHz. L_{dio} and $L_d + L_s$ are measured by time domain reflectometry (TDR) method. It is difficult to separate L_d and

L_s[104], and hence, they are divided into two: L_s = 4 nH and L_d = 4 nH. L_N is obtained by electromagnetic simulation.

The geometry of the bus bar is shown in Fig. 5.6. The thickness and height are set to 0.105 mm and 1.6 mm, respectively, to compare with Fig. 5.5(c), which satisfies the design objective. There is a wire for the AC current probe, P6022 (Tektronix, 120 MHz), between the diode and MOSFET. The input voltage and output current are set to 400 V and 30 A, respectively.

5.3.2 Experimental result

Table 5.5 lists the objective functions of the simulation and experiments. It is clear that the simulation results are in good agreement with the measured results. Fig. 5.7 shows an experimental switching waveform.

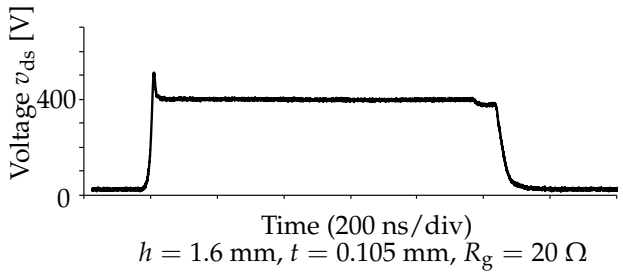
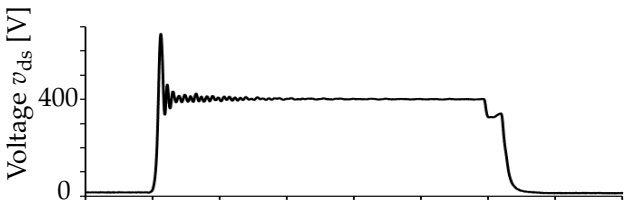


FIGURE 5.7: Experimental switching waveform which satisfies the design objective.



(a) $h = 5.2$ mm, $t = 0.8$ mm, $R_g = 10\ \Omega$

Time (200 ns/div)

FIGURE 5.8: Experimental switching waveforms which do not satisfy the design objective.

On the other hand, this proposed method is able to predict bad designs as well. Fig. 5.8 shows the bad cases whose surge voltage or damped oscillation level is high for example. This case indicates that there is a possibility to design the bad case waveform without the proposed method.

TABLE 5.4: Power devices for experimentation.

Device	SiC MOSFET	SiC SBD
Manufacturer	Rohm	Rohm
Model	SCT2280KE	SCS205KG
Package	TO-247-3	TO-220-2
Voltage rating	1,200 V	1,200 V
Current rating (pulse)	35 A	80 A

TABLE 5.5: Experimental objective function

	Simulation	Experiments
V_{sn}	0.444	0.868
V_{rn}	0.318	0.503
e_{obj}	0.546	1.003

5.4 Expansion of the design method

The proposed design method is able to expand towards not only the surge voltage and oscillation evaluation but also the switching loss, etc. Because the evaluated items are normalized to equally evaluate them, other items can be evaluated in the same manner. This chapter adds the switching loss evaluation as an example into the evaluated items discussed in the previous sections.

If neither the surge voltage nor damped oscillation cannot be suppressed simultaneously by designing the parasitic parameters of the bus bar, then the gate resistor has to be large to suppress both the surge voltage and damped oscillation. However, the large gate resistance makes the switching loss large; thus, the gate resistance needs to be designed to be as small as possible. The switching loss is then considered as a parameter to evaluate the switching waveform. The switching loss is the sum of the turn-off loss W_{off} and turn-on loss W_{on}:

$$W = W_{\mathrm{off}} + W_{\mathrm{on}} \tag{5.6}$$

The switching loss can also be normalized as follows:

$$W_{\mathrm{n}} = \frac{W - W_{\mathrm{min}}}{W_{\mathrm{des}} - W_{\mathrm{min}}} \tag{5.7}$$

where W is the switching loss, W_{min} is the minimal value obtained in the simulation, and W_{des} is the design objective. If the switching loss obtained in the simulation is equal to the minimal value, the normalized switching loss becomes zero. If the switching loss obtained in the simulation is equal to the design objective, the normalized switching loss becomes one.

To consider the surge voltage, damped oscillation, and switching loss simultaneously, the objective function is as given below:

$$e_{\mathrm{obj}} = \sqrt{V_{\mathrm{sn}}^2 + V_{\mathrm{rn}}^2 + W_{\mathrm{n}}^2} \tag{5.8}$$

The laminated busbar geometry can be considered as a good design when all the normalized values are within one and objective function is located near origin.

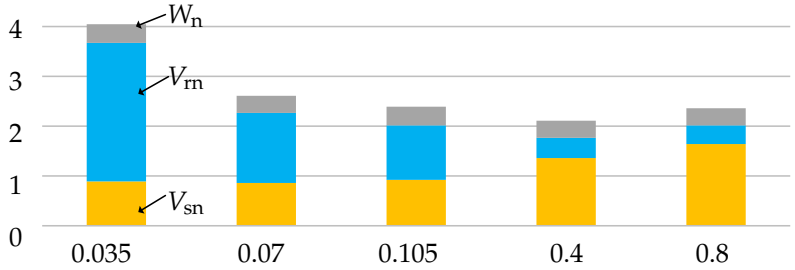
Table 5.6 shows the swept variables. The difference from the previous section is the gate resistor. From this condition, the simulation based on Fig. 5.3 is performed.

Figure 5.9 shows the breakdown of the normalized values from the simulation results. It is evident that the switching loss heavily depends on the gate resistor. This is because of the switching speed reduction caused by the increase in the gate resistor. Also, the level of the surge voltage and damped oscillation reduces as the gate resistor increases. This phonomena is able to be described by switching speed reduction. As the busbar thickness increases, the surge voltage level increases, while the damped oscillation level decreases. It must be noted that the lowest value of the objective function has a different geometry depending on the gate resistor. When the gate resistor is 10 Ω, the busbar thickness must be 0.4 mm, while the busbar thickness must be 0.105 mm when the gate resistor is 20 Ω. This indicates that the busbar geomtery with the lowest value of objective function depends on the switching speed.

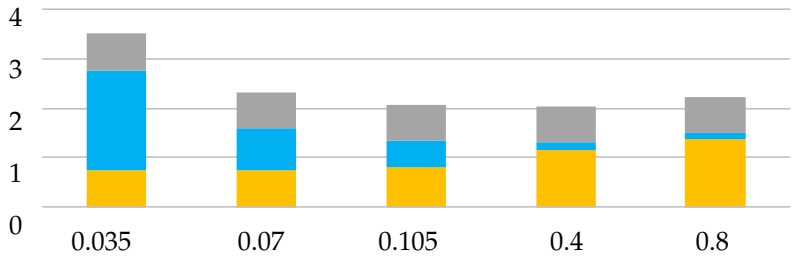
The switching loss is able to be considered since the proposed method deals with the normalized value which does not require the same unit or same order of value. The ability to include other evaluated items has been validated from this example. This enables the circuit designer to aquire the wide range of design space of the laminated busbar.

TABLE 5.6: Swept variables.

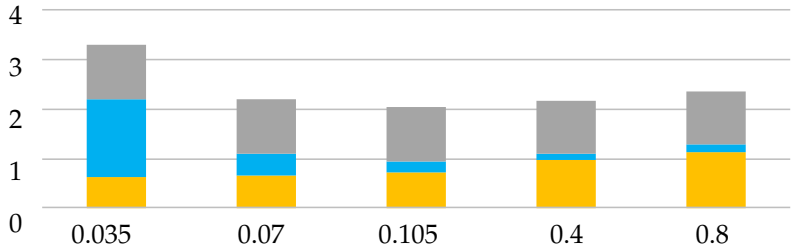
	t	h	R_g
Minimum value	0.035 mm	0.4 mm	10 Ω
Maximum value	0.8 mm	5.2 mm	100 Ω



(a) $h = 1.6$ mm, $R_g = 10\ \Omega$



(b) $h = 1.6$ mm, $R_g = 20\ \Omega$



(c) $h = 1.6$ mm, $R_g = 30\ \Omega$

Horizontal axis: bus bar thickness t [mm]

Vertical axis: evaluated items

FIGURE 5.9: Relationship between objective functions breakdown and gate resistor.

5.5 Summary

In this chapter, it was clear that the bus bar geometry affects the switching waveforms so an design procedure has been proposed. Designed bus bars were achieved,

and it is detected that there is a minimum point of the objective function by changing bus bar geometry. The simulation results have been verified by comparing the experimental results with that of the buck chopper circuit. As a result, it is necessary to design both the bus bar structure and gate resistor using this design procedure to satisfy all of the design values of the surge voltage and damped oscillation. This method is verified as the solution to handle the issues caused by high-speed switching. The normalization is able to include other evaluated items based on the design specification. For example, while the oscillation of the low-side MOSFET is evaluated in this chapter, the oscillation of the high-side diode can be added to the objective function as well. The author has confirmed this expandability to include the switching loss with the surge voltage and oscillation.

Chapter 6

Conclusion and Future Work

6.1 Conclusion

This section concludes the whole previous chapters.

In Chapter 1, the high-speed switching with WBG devices are discussed on the basis of the recent power electroncis background. The high-speed switching has both advantages and disadvantages, and the disadvantages are actively overcome by many studies. In those studies, a laminated busbar with focus only on just low inductance were examined. However, other aspects are herein discussed from the perspective of the design method of the laminated busbar geometry.

In Chapter 2, the issues related to high-speed switching and laminated busbar are revealed. Each issue is defined to be quantitatively evaluated. To solve those issues using the laminated busbar, the parasitic parameters including the frequency characteristics are discussed.

Chapter 3 addresses the current imbalance issue. The aperture size is the most critical geometry in the busbar, and the design procedure of the aperture size is illustrated.

Chapter 4 presents the solution of the oscillation issue. This includes the parasitic conductance, which is the most important component to design the damped characteristics, and the verification of its design method. The notable aspect is the evaluation of the damped oscillation in the time domain, which no prior study has reported.

In Chapter 5, the integration of the design method of damped oscillation into the conventional surge voltage design is detailed. To equivalently evaluate the items

have different units, normalization is proposed. The verification of the laminated busbar design method for high-speed switching on the basis of the design procedure is presented.

The findings of this study can be applied to not only high-speed switching technologies, but also to conventional switching speed. As mentioned in Chapter 2, the switching speed and the wavelength are related; the applied range of this design method is depicted in Fig. 6.1. This method can also be applied in GaN power devices if the switching speed is within the range shown in Fig. 6.1, and the system employs the laminated busbars for connection of components.

	Switching time		
	1 ns - 10 ns	10 ns - 30 ns	30 ns - 100 ns
Busbar length			
1 mm - 10 mm	◎	◎	○
10 mm - 100 mm	◎	◎	◎
100 mm - 200 mm	×	○	◎
200 mm - 1000 mm	×	×	◎

FIGURE 6.1: Compartmentalization of the laminated busbar design method.

6.2 Future work

6.2.1 Design automation for power electronics

Design Automation for Power Electronics (DAPE) has been undergoing development from the start of DAPE conference in 2020. The research field of DAPE expands the power electronics field to various fields such as artificial intelligence, computational automated design, and real-time hardware simulationc [105]. The busbar relevant technology is also one of the candidates in the design automation components. The author has proposed the neural-network-based busbar model. The accuracy increases as the number of datasets increase. Fig. 6.2 shows the schematic of a neural network to predict the parasitic parameters from geometry inputs. Once the model is constructed, the calculation cost must decrease compared with that of the electromagnetic simulation. This model can be inserted in the design automation schematic as shown in Fig. 6.3. The flowchart shows simultaneous software and hardware

simulation. Here, the software is the active gate driver (AGD) pattern, and the hardware is the laminated busbar. Fig.6.3 shows the optimization flowchart, which is considered as a future work to be based on this dissertation. To test the concept, the surge voltage, loss, and electromagnetic noise are optimized during power device switching by using the busbar insulation thickness t_{ins} as the hardware and the AGD pattern as the software decision variables. The optimization algorithm used is particle swarm optimization (PSO). The flowchart is divided into four phases, as follows:

(1) Updating the decision variables;

(2) predicting the parasitic parameter frequency response from the variables related to the structure among the decision variables;

(3) performing circuit simulation; and

(4) calculation of the objective function from simulation results

At the beginning of the simulation, both initial and random values determined by the user are entered into the decision variables (flowchart (1)), and Flowcharts (2) through (4) are then executed. If the objective function calculated in (4) exceeds the required value, the decision variable is updated by returning to Flowchart (1). This calculation is repeated to minimize the objective function. To observe the process of optimization, the required value is set to minimum, and the calculation is performed for a given number of trials.

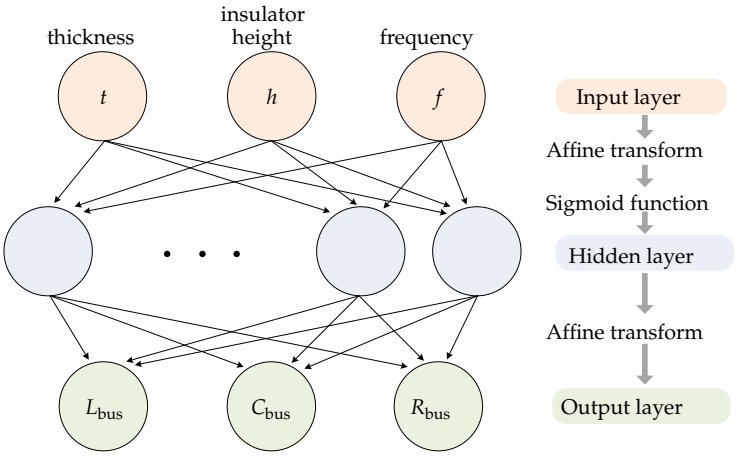


FIGURE 6.2: Neural network layers.

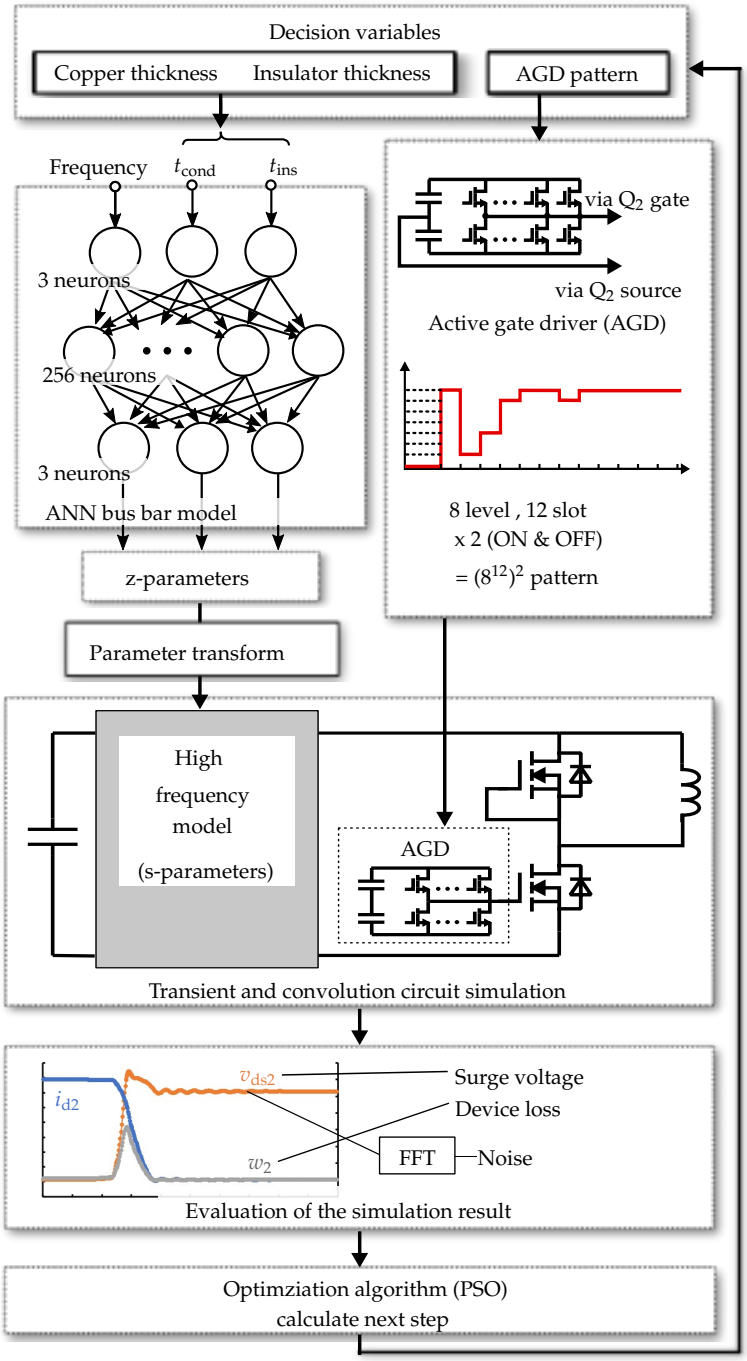
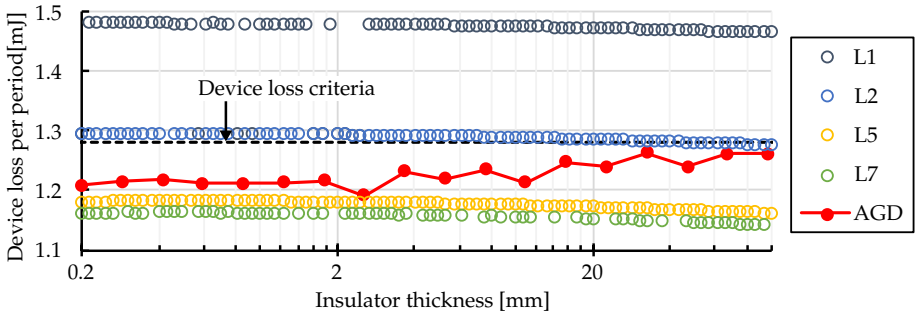


FIGURE 6.3: Design automation flow chart.

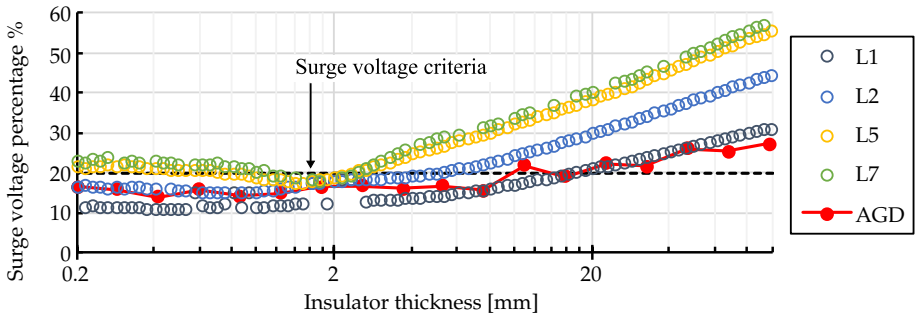
Fig. 6.4 shows the simulation results. From top to bottom, the switching loss, surge votlage, and damped oscillation level are simulated. L1 - L7 are the level of the gate resistor; L1 is the largest gate resistor in this condition, and L7 is the smallest gate resistor value. The red solid lines in Fig. 6.4 are the respective evaluated values when AGD is operated. The device loss in Fig. 6.4(a) can achieve the target value at an insulation thickness of t_{ins} in the analysis range. The surge voltage in Fig. 6.4(b)

meets the target value in the range of $t_{\mathrm{ins}} \leq 18.5$ mm. This result is equivalent to that associated with L1 and L2 without AGD and is reduced on average by 38% when compared to that associated with L7. The noise voltage in Fig.6.4(c) satisfies the target value in the analysis range.

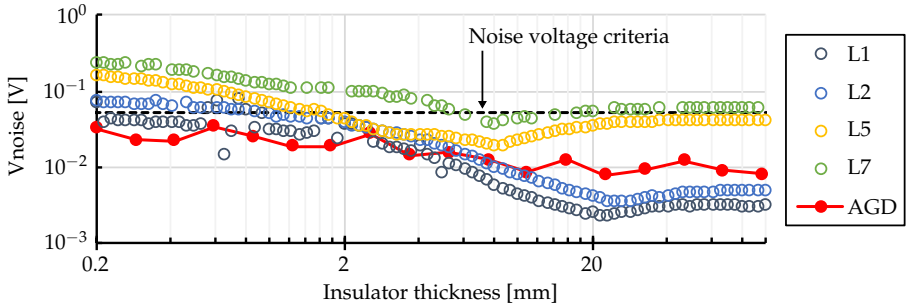
Finally, the optimal solution was the AGD pattern at insulation thickness $t_{\mathrm{ins}} =$ 1.23 mm. Fig. 6.5 shows the design space of the insulation thickness.



(a) Device loss per a switch and insulator thickness.



(b) Surge voltage percentage and insulator thickness.



(c) Noise voltage and insulator thickness.

FIGURE 6.4: Comparison of the objective items with and without AGD.

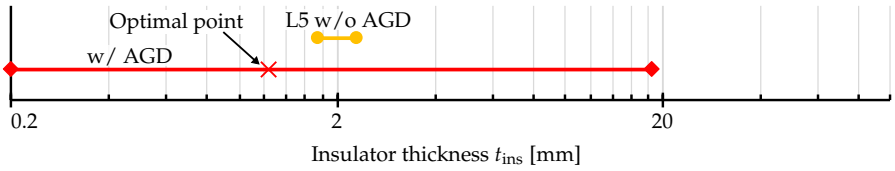


FIGURE 6.5: The design space of insulator thickness with and without AGD.

The main components such as inductors have been widely investigated and developed. However, there is a paucity of studies that seek to apply the busbar into design automation. This dissertation demonstrates the impact of the laminated busbar design, and hence, this technology will be expanded to these field in the near future.

6.2.2 Electromagnetic radiation

The busbar has a certain length ranging from several tens of mm to several hundreds of mm. In this context, the busbar can work as an anntena at giga hertz region. This dissertation scopes the frequency range from DC to 100 MHz to handle the busbar as constant passive components. However, the rectangular or trapezoidal waveforms such as drain current must have higher frequency components. If the switching speed increases significantly, in such range of frequency, the electromagnetic noise must increase. In such a situation, the busbar may form the resonance path, and the standing wave of current may flows on the busbar at several giga hertz range. Some busbar designs have a slit for current distribution sharing, resulting in the electromagnetic radiation as the slit works as a slot anntena. Fig. 6.6 shows the example of the slit for current sharing. This slot is one of the solutions for sharing the current for multiple devices; however, this method may make the electromagnetic environment harsh if the high-speed switching is applied.

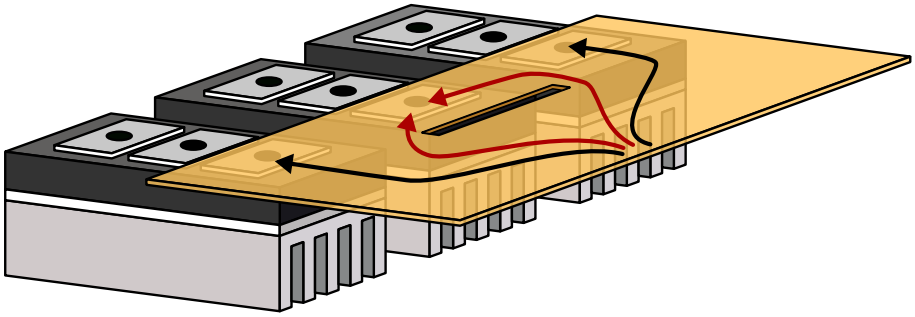


FIGURE 6.6: The slit on a busbar for the parasitic inductance equalization.

This issue may be examined in the future research concering the laminated busbar and high-speed switching issues.

Bibliography

[1] "ADOPTION OF THE PARIS AGREEMENT," United Nations / Framework Convention on Climate Change, Paris, An Official Publication, 2015.

[2] "Strategic Energy Plan," Ministry of Economy, Trade and Industry, White Paper, 2018. [Online]. Available: https://www.enecho.meti.go.jp/en/category/others/basic_plan/.

[3] "The Long-term Strategy under the Paris Agreement," Ministry of Economy, Trade and Industry, Government Report, 2019.

[4] Kyushu Electric Power, " 九州本土における再エネ出力制御の実施状況について," Ministry of Economy, Trade and Industry, Government Report, 2019.

[5] "Global EV Outlook 2019," IEA, Tech. Rep., 2019.

[6] "Waypoint 2050," Air Transport Action Group, Tech. Rep., 2021. [Online]. Available: https://aviationbenefits.org/environmental-efficiency/climate-action/waypoint-2050/.

[7] " 電動推進航空機の最新動向," International Aircraft Development Fund (IADF), Tech. Rep., 2018.

[8] G. Buticchi, S. Bozhko, M. Liserre, P. Wheeler, and K. Al-Haddad, "On-Board Microgrids for the More Electric Aircraft—Technology Review," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 7, pp. 5588–5599, 2019. DOI: 10.1109/TIE.2018.2881951.

[9] E. A. Grunditz and T. Thiringer, "Performance analysis of current bevs based on a comprehensive review of specifications," *IEEE Transactions on Transportation Electrification*, vol. 2, no. 3, pp. 270–289, 2016. DOI: 10.1109/TTE.2016.2571783.

[10] S. Chakraborty, H.-N. Vu, M. M. Hasan, D.-D. Tran, M. E. Baghdadi, and O. Hegazy, "Dc-dc converter topologies for electric vehicles, plug-in hybrid electric vehicles and fast charging stations: State of the art and future trends," *Energies*, vol. 12, no. 8, 2019.

[11] M. Noriko, T. Michiya, and O. Hitoshi, "Moving to an All-Electric Aircraft System," IHI Ltd., Tech. Rep. 1, 2014.

[12] H. Schefer, L. Fauth, T. H. Kopp, R. Mallwitz, J. Friebe, and M. Kurrat, "Discussion on Electric Power Supply Systems for All Electric Aircraft," *IEEE Access*, vol. 8, pp. 84 188–84 216, 2020. DOI: 10.1109/ACCESS.2020.2991804.

[13] A. Nawawi, C. F. Tong, S. Yin, *et al.*, "Design and Demonstration of High Power Density Inverter for Aircraft Applications," *IEEE Transactions on Industry Applications*, vol. 53, no. 2, pp. 1168–1176, 2017. DOI: 10.1109/TIA.2016.2623282.

[14] J. Welstead, J. Felder, M. Guynn, *et al.*, "Overview of the NASA STARC-ABL (Rev. B) Advanced Concept," Air Transport Action Group, Tech. Rep., 2021. [Online]. Available: https://aviationbenefits.org/environmental-efficiency/climate-action/waypoint-2050/.

[15] I. Laird, X. Yuan, J. Scoltock, and A. J. Forsyth, "A Design Optimization Tool for Maximizing the Power Density of 3-Phase DC-AC Converters Using Silicon Carbide (SiC) Devices," *IEEE Transactions on Power Electronics*, vol. 33, no. 4, pp. 2913–2932, 2018. DOI: 10.1109/TPEL.2017.2705805.

[16] K. Yamaguchi, K. Katsura, T. Yamada, and Y. Sato, "High Power Density SiC-Based Inverter with a Power Density of 70 kW/liter or 50 kW/kg," *IEEJ Journal of Industry Applications*, vol. 8, no. 4, pp. 694–703, 2019. DOI: 10.1541/ieejjia.8.694.

[17] Z. Liu, F. C. Lee, Q. Li, and Y. Yang, "Design of GaN-Based MHz Totem-Pole PFC Rectifier," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 799–807, 2016. DOI: 10.1109/JESTPE.2016.2571299.

[18] J. Hu, J. Wang, R. Burgos, B. Wen, and D. Boroyevich, "High-Density Current-Transformer-Based Gate-Drive Power Supply With Reinforced Isolation for

10-kV SiC MOSFET Modules," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 3, pp. 2217–2226, 2020. DOI: 10.1109/JESTPE.2019.2943742.

[19] A. Stratta, D. Gottardo, M. D. Nardo, *et al.*, "Optimal integrated design of a magnetically coupled interleaved h-bridge," *IEEE Transactions on Power Electronics*, vol. 37, no. 1, pp. 724–737, 2022. DOI: 10.1109/TPEL.2021.3094025.

[20] B. Zhang and S. Wang, "A survey of emi research in power electronics systems with wide-bandgap semiconductor devices," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 626–643, 2020. DOI: 10.1109/JESTPE.2019.2953730.

[21] A. M. Naradhipa, S. Kim, D. Yang, S. Choi, I. Yeo, and Y. Lee, "Power density optimization of 700 khz gan-based auxiliary power module for electric vehicles," *IEEE Transactions on Power Electronics*, vol. 36, no. 5, pp. 5610–5621, 2021. DOI: 10.1109/TPEL.2020.3026328.

[22] J. Biela, U. Badstuebner, and J. W. Kolar, "Impact of power density maximization on efficiency of dc–dc converter systems," *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 288–300, 2009. DOI: 10.1109/TPEL.2009.2006355.

[23] B. Wang, N. Tipirneni, M. Riva, *et al.*, "An efficient high-frequency drive circuit for gan power hfets," *IEEE Transactions on Industry Applications*, vol. 45, no. 2, pp. 843–853, 2009. DOI: 10.1109/TIA.2009.2013578.

[24] J. W. Kolar, U. Drofenik, J. Biela, *et al.*, "Pwm converter power density barriers," in *2007 Power Conversion Conference - Nagoya*, 2007, P–9–P–29. DOI: 10.1109/PCCON.2007.372914.

[25] J. D. van Wyk and F. C. Lee, "On a future for power electronics," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 1, no. 2, pp. 59–72, 2013. DOI: 10.1109/JESTPE.2013.2271499.

[26] T. Kimura, R. Saitou, K. Kubo, K. Nakatsu, H. Ishikawa, and K. Sasaki, "High-power-density inverter technology for hybrid and electric vehicle applications," *Hitachi Review*, vol. 63, no. 2, pp. 96–102, 2014.

[27] E. Gurpinar and A. Castellazzi, "Single-phase t-type inverter performance benchmark using si igbts, sic mosfets, and gan hemts," *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7148–7160, 2016. DOI: 10.1109/TPEL.2015.2506400.

[28] Z. S. Du, P. Channegowda, P. Kshirsagar, and S. Dwari, "High density high power dc-dc converter architectures for future electric transportation applications," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 5862–5869. DOI: 10.1109/ECCE.2019.8913313.

[29] A. Deshpande, A. Imran, R. Paul, Z. Yuan, H. Peng, and F. Luo, "High power density 1700-v/ 300-a si-igbt and sic-mosfet hybrid switch-based half-bridge power module," in *2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2020, pp. 3979–3986. DOI: 10.1109/ECCE44975.2020.9236124.

[30] Y. Zhang, C. Yao, X. Zhang, H. Chen, H. Li, and J. Wang, "Power loss model for gan-based mhz critical conduction mode power factor correction circuits," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. PP, pp. 1–1, Oct. 2019. DOI: 10.1109/JESTPE.2019.2948148.

[31] J. Chen, X. Du, Q. Luo, X. Zhang, P. Sun, and L. Zhou, "A Review of Switching Oscillations of Wide Bandgap Semiconductor Devices," *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13 182–13 199, 2020. DOI: 10.1109/TPEL.2020.2995778.

[32] F. C. Lee, S. Wang, and Q. Li, "Next generation of power supplies—design for manufacturability," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 6, pp. 6462–6475, 2021. DOI: 10.1109/JESTPE.2020.3002857.

[33] F. Savi, D. Barater, M. D. Nardo, *et al.*, "High-speed electric drives: A step towards system design," *IEEE Open Journal of the Industrial Electronics Society*, vol. 1, pp. 10–21, 2020. DOI: 10.1109/OJIES.2020.2973883.

[34] A. Poorfakhraei, M. Narimani, and A. Emadi, "A review of multilevel inverter topologies in electric vehicles: Current status and future trends," *IEEE*

Open Journal of Power Electronics, vol. 2, pp. 155–170, 2021. DOI: 10.1109/OJPEL.2021.3063550.

[35] K. Wang, X. Yang, H. Li, H. Ma, X. Zeng, and W. Chen, "An analytical switching process model of low-voltage egan hemts for loss calculation," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 635–647, 2016. DOI: 10.1109/TPEL.2015.2409977.

[36] D. Han, C. T. Morris, W. Lee, and B. Sarlioglu, "A case study on common mode electromagnetic interference characteristics of gan hemt and si mosfet power converters for ev/hevs," *IEEE Transactions on Transportation Electrification*, vol. 3, no. 1, pp. 168–179, 2017. DOI: 10.1109/TTE.2016.2622005.

[37] S. Tiwari, O.-M. Midtgård, and T. M. Undeland, "Design of low inductive busbar for fast switching SiC modules verified by 3D FEM calculations and laboratory measurements," in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, 2016, pp. 1–8. DOI: 10.1109/COMPEL.2016.7556689.

[38] A. Okubo, K. Throngnumchai, and T. Hayashi, "Common mode EMI reduction structure of EV/HEV inverters for high-speed switching," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 2341–2345. DOI: 10.1109/ECCE.2017.8096454.

[39] N. Oswald, P. Anthony, N. McNeill, and B. H. Stark, "An Experimental Investigation of the Tradeoff between Switching Losses and EMI Generation With Hard-Switched All-Si, Si-SiC, and All-SiC Device Combinations," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2393–2407, 2014. DOI: 10.1109/TPEL.2013.2278919.

[40] Z. Wang, M. Chinthavali, S. L. Campbell, T. Wu, and B. Ozpineci, "A 50-kW Air-Cooled SiC Inverter With 3-D Printing Enabled Power Module Packaging Structure and Genetic Algorithm Optimized Heatsinks," *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 6256–6265, 2019. DOI: 10.1109/TIA.2019.2938471.

[41] P. Nayak and K. Hatua, "Parasitic Inductance and Capacitance-Assisted Active Gate Driving Technique to Minimize Switching Loss of SiC MOSFET," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 10, pp. 8288–8298, 2017. DOI: 10.1109/TIE.2017.2711512.

[42] K. Yamaguchi, K. Katsura, T. Yamada, and Y. Sato, "Comprehensive Study on Gate Driver for SiC-MOSFETs with Gate Boost," *IEEJ Journal of Industry Applications*, vol. 7, no. 3, pp. 218–228, 2018. DOI: 10.1541/ieejjia.7.218.

[43] 野口 季彦, 水野 知博, and 村田 宗洋, " スイッチングアシスト補助回路を用いたMOSFETの高速スイッチング法," 電気学会論文誌D（産業応用部門誌）, vol. 133, no. 12, pp. 1186–1192, 2013. DOI: 10.1541/ieejias.133.1186.

[44] Rohm Semiconductor, "R6020PNJ," Datasheet, May 2019, [Accessed: Mar 21, 2022]. [Online]. Available: https://www.rohm.co.jp/products/mosfets/automotive/high-voltage/r6020pnjfra-product.

[45] Rohm Semiconductor, "SCT3120AL Datasheet," Datasheet, Jun. 2018, [Accessed: Oct. 26th, 2022]. [Online]. Available: https://www.rohm.com/products/sic-power-devices/sic-mosfet/sct3120al-product.

[46] P. Wang, L. Zhang, X. Lu, H. Sun, W. Wang, and D. Xu, "An Improved Active Crosstalk Suppression Method for High-Speed SiC MOSFETs," *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 7736–7744, 2019. DOI: 10.1109/TIA.2019.2916302.

[47] H.-F. Huang, L.-Y. Deng, B.-J. Hu, and G. Wei, "Techniques for Improving the High-Frequency Performance of the Planar CM EMI Filter," *IEEE Transactions on Electromagnetic Compatibility*, vol. 55, no. 5, pp. 901–908, 2013. DOI: 10.1109/TEMC.2013.2240392.

[48] P. Hofstetter and M.-M. Bakran, "Mitigating Drain Source Voltage Oscillation for SiC Power MOSFETs in order to reduce Electromagnetic Interference," in *2019 21st European Conference on Power Electronics and Applications*, 2019. DOI: 10.23919/EPE.2019.8914884.

[49] C. Yao, P. Yang, H. Chen, *et al.*, "Electromagnetic Noise Mitigation for Ultrafast on-Die Temperature Sensing in High-Power Modules," *IEEE Transactions*

on Power Electronics, vol. 33, no. 2, pp. 1178–1187, 2018. DOI: 10.1109/TPEL.2017.2688334.

[50] T. Cui, Q. Ma, P. Xu, and Y. Wang, "Analysis and Optimization of Power MOSFETs Shaped Switching Transients for Reduced EMI Generation," *IEEE Access*, vol. 5, pp. 20 440–20 448, 2017. DOI: 10.1109/ACCESS.2017.2758443.

[51] P. Nayak and K. Hatua, "Active Gate Driving Technique for a 1200 V SiC MOSFET to Minimize Detrimental Effects of Parasitic Inductance in the Converter Layout," *IEEE Transactions on Industry Applications*, vol. 54, no. 2, pp. 1622–1633, 2018. DOI: 10.1109/TIA.2017.2780175.

[52] Z. Wang, Y. Wu, M. H. Mahmud, Z. Yuan, Y. Zhao, and H. A. Mantooth, "Busbar Design and Optimization for Voltage Overshoot Mitigation of A Silicon Carbide High-Power Three-Phase T-Type Inverter," *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 204–214, 2021. DOI: 10.1109/TPEL.2020.2998465.

[53] G. Engelmann, A. Sewergin, M. Neubert, and R. W. D. Doncker, "Design Challenges of SiC Devices for Low- and Medium-Voltage DC-DC Converters," *IEEJ Journal of Industry Applications*, vol. 8, no. 3, pp. 505–511, 2019. DOI: 10.1541/ieejjia.8.505.

[54] T. Yanagi, H. Sakairi, H. Otake, *et al.*, "Circuit Simulation of a Silicon-Carbide MOSFET Considering the Effect of the Parasitic Elements on Circuit Boards by Using S-parameters," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, San Antonio, TX, USA, 2018, pp. 2875–2878. DOI: 10.1109/APEC.2018.8341425.

[55] B. Zhang and S. Wang, "Parasitic Inductance Modeling and Reduction for Wire-Bonded Half-Bridge SiC Multichip Power Modules," *IEEE Transactions on Power Electronics*, vol. 36, no. 5, pp. 5892–5903, 2021. DOI: 10.1109/TPEL.2020.3032521.

[56] H. Gui, R. Chen, J. Niu, *et al.*, "Design of Low Inductance Busbar for 500 kVA Three-Level ANPC Converter," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 112–115. DOI: 10.1109/ECCE.2019.8912605.

[57] Y. Zhang, K. Dai, H. Xu, *et al.*, "DSP-Based SiC-MOSFET SAPF With 100-kHz Sampling and Switching Frequency for Wideband Harmonic Suppression," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 1, pp. 689–701, 2021. DOI: 10.1109/JESTPE.2020.2982408.

[58] M. C. Caponet, F. Profumo, R. W. D. Doncker, and A. Tenconi, "Low Stray Inductance Bus Bar Design and Construction for Good EMC Performance in Power Electronics Circuits," *IEEE Transactions on Power Electronics*, vol. 17, no. 2, pp. 225–231, 2002. DOI: 10.1109/63.988833.

[59] D. O. Thomas, M. Sylvain, G. Jean-Michel, J.-L. Schanen, and A. Perregaux, "Reduction of conducted EMC using busbar stray elements," in *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, 2009, pp. 2028–2033. DOI: 10.1109/APEC.2009.4802952.

[60] S. Negri, X. Wu, X. Liu, F. Grassi, G. Spadacini, and S. A. Pignari, "Mode Conversion in DC-DC Converters with Unbalanced Busbars," in *2019 Joint International Symposium on Electromagnetic Compatibility, Sapporo and Asia-Pacific International Symposium on Electromagnetic Compatibility (EMC Sapporo/APEMC)*, 2019, pp. 112–115. DOI: 10.23919/EMCTokyo.2019.8893915.

[61] M. Xu, N. Wang, and Z. Wang, "Optimized design of laminated busbar for large-capacity back-to-back converters," *Energies*, vol. 15, no. 3, 2022, Article number = 774, ISSN: 1996-1073. DOI: 10.3390/en15030774. [Online]. Available: https://www.mdpi.com/1996-1073/15/3/774.

[62] C. Chen, X. Pei, Y. Shi, X. Lin, X. Liu, and Y. Kang, "Modeling and optimization of high power inverter three-layer laminated busbar," in *2012 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2012, pp. 1380–1385. DOI: 10.1109/ECCE.2012.6342654.

[63] A. Deshpande, Y. Chen, B. Narayanasamy, Z. Yuan, C. Chen, and F. Luo, "Design of a High-Efficiency, High Specific-Power Three-Level T-Type Power Electronics Building Block for Aircraft Electric-Propulsion Drives," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 407–416, 2020. DOI: 10.1109/JESTPE.2019.2952367.

[64] L. Ravi, X. Lin, D. Dong, and R. Burgos, "A 16 kV PCB-Based DC-Bus Distributed Capacitor Array with Integrated Power-AC-Terminal for 10 kV SiC MOSFET Modules in Medium-Voltage Inverter Applications," in *Proceedings on 2020 IEEE Energy Conversion Congress and Exposition (ECCE)*, Detroit, MI, USA, Oct. 2020, pp. 3998–4005. DOI: 10.1109/ECCE44975.2020.9236300.

[65] S. Srdic, C. Zhang, and S. Lukic, "A low-inductance Sectional Busbar for Snuberless Operation of SiC-based EV Traction Inverters," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 6805–6809. DOI: 10.1109/ECCE.2019.8912204.

[66] J. Schanen, E. Clavel, and J. Roudet, "Modeling of low inductive busbar connections," *IEEE Industry Applications Magazine*, vol. 2, no. 5, pp. 39–43, 1996. DOI: 10.1109/2943.532153.

[67] F. Zare and G. Ledwich, "Reduced layer planar busbar for voltage source inverters," *IEEE Transactions on Power Electronics*, vol. 17, no. 4, pp. 508–516, 2002. DOI: 10.1109/TPEL.2002.800990.

[68] H. Wen and W. Xiao, "Design and optimization of laminated busbar to reduce transient voltage spike," in *2012 IEEE International Symposium on Industrial Electronics*, 2012, pp. 1478–1483. DOI: 10.1109/ISIE.2012.6237309.

[69] D. Cottet, I. Stevanovic, B. Wunsch, D. Daroui, J. Ekman, and G. Antonini, "EM Simulation of Planar Bus Bars in Multi-Level Power Converters," in *2012 International Symposium on Electromagnetic Compatibility*, 2012, pp. 1–6. DOI: 10.1109/EMCEurope.2012.6396765.

[70] A. Hino and K. Wada, "Analysis of the Stray Inductance of Laminated Bus Bar for Parallel Connected Capacitors, 直流側コンデンサの並列接続時におけるラミネートバスバーのインダクタンス解析手法に関する検討," in 平成*26*年電気学会全国大会, Article number = 4-033, 2014, pp. 52–53.

[71] T. Hirao, K. Wada, and T. Shimizu, "Circulating resonant current between integrated half-bridge modules with capacitor for inverter circuit using SiC-MOSFET," in *2016 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2016, pp. 1–7. DOI: 10.1109/ECCE.2016.7854916.

[72] J. Wang, S. Yu, and X. Zhang, "Effect of Key Physical Structures on the Laminated Bus Bar Inductance," in *2016 IEEE 8th International Power Electroncis and Motion Control Conference (IPEMC-ECCE Asia)*, 2016, pp. 3689–3694. DOI: 10.1109/IPEMC.2016.7512886.

[73] J. Stewart, J. Neely, J. Delhotal, and J. Flicker, "DC link bus design for high frequency, high temperature converters," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2017, pp. 809–815. DOI: 10.1109/APEC.2017.7930789.

[74] B. Aberg, R. S. K. Moorthy, L. Yang, W. Yu, and I. Husain, "Estimation and minimization of power loop inductance in 135 kw sic traction inverter," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 1772–1777. DOI: 10.1109/APEC.2018.8341257.

[75] P. B. T. Singh, P. B. Bobba, K. Suresh, and B. J. Varghere, "Extensive review on Laminated bus bar for low and high power applications," in *1st International Conference on Sustainable Energy and Future Electric Transportation (SeFet 2019)*, Article Number=01009, vol. 87, E3S Web of Conference, 2019. DOI: 10.1051/e3sconf/20198701009.

[76] A. Venugopal and F. Robert, "Influence of Physical Parameters on the Capacitance of Laminated Busbars for Electric Vehicles," *Journal of Physics: Conference Series*, vol. 2335, 2022, Article number = 012046. DOI: 10.1088/1742-6596/2335/1/012046.

[77] Z. Yuan, Y. Wang, Z. Wang, *et al.*, "Insulation and Switching Performance Optimization for Partial-Discharge-Free Laminated Busbar in More-Electric Aircraft Applications," *IEEE Transactions on Power Electronics*, vol. 37, no. 6, pp. 6831–6843, 2022.

[78] Z. Lounis, I. Rasoanarivo, and B. Davat, "Minimization of wiring inductance in high power IGBT inverter," *IEEE Transactions on Power Delivery*, vol. 15, no. 2, pp. 551–555, 2000. DOI: 10.1109/61.852983.

[79] C. Chen, X. Pei, Y. Chen, and Y. Kang, "Investigation, Evaluation, and Optimization of Stray Inductance in Laminated Busbar," *IEEE Transactions on*

Power Electronics, vol. 29, no. 7, pp. 3679–3693, 2014. DOI: 10.1109/TPEL.2013.2282621.

[80] Z. Yuan, H. Peng, A. Deshpande, *et al.*, "Design and Evaluation of Laminated Busbar for Three-Level T-Type NPC Power Electronics Building Block With Enhanced Dynamic Current Sharing," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 395–406, 2020. DOI: 10.1109/JESTPE.2019.2947488.

[81] D. Wang, M. Preindl, F. Peng, J. Ye, and A. Emadi, "DC-Bus Design with Hybrid Capacitor Bank in Single-Phase PV Inverters," in *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, Beijing, China, Oct. 2017, pp. 2425–2430. DOI: 10.1109/IECON.2017.8216408.

[82] S. Zhao and W. Chou, "Analytic Model of the Voltage Oscillation in a Power Conversion System with DC-Link Capacitors," in *2021 IEEE Energy Conversion Congress and Exposition*, 2021, pp. 5554–5560. DOI: 10.1109/ECCE47101.2021.9595713.

[83] Z. Liang, S. Hu, M. Wang, and X. He, "DC-Link Busbar Network Design and Evaluation Method for the Large-Capacity Power Electronic Converter," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 9, no. 4, pp. 4137–4145, 2021. DOI: 10.1109/JESTPE.2021.3073513.

[84] R. Alizadeh, M. Schupbach, T. Adamson, *et al.*, "Busbar Design for Distributed DC-Link Capacitor Banks for Traction Applications," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Portland, OR, USA, Sep. 2018, pp. 4810–4815. DOI: 10.1109/ECCE.2018.8558380.

[85] H. Wang and F. Blaabjerg, "Reliability of Capacitors for DC-Link Applications — An Overview," *IEEE Transactions on Industry Applications*, vol. 50, no. 5, pp. 3569–3578, 2014. DOI: 10.1109/TIA.2014.2308357.

[86] S.-I. Hayashi and K. Wada, "Implementation of a Gate Drive Circuit for Reducing Switching Loss and Surge Voltage," *IEEJ Transactions on Industry Applications*, vol. 136, no. 10, pp. 791–797, 2016. DOI: 10.1541/ieejias.136.791.

[87] R. Shirai and T. Shimizu, "Time Domain Analysis of Transmission Failure on CAN System due to Differential-Mode Noise Emitted from a Buck Converter," *IEEJ Journal of Industry Applications*, vol. 8, no. 4, pp. 608–614, 2019. DOI: 10.1541/ieejjia.8.608.

[88] B. Hafez, A. S. Abdel-Khalik, A. M. Massoud, S. Ahmed, and R. D. Lorenz, "Single-Sensor-Based Three-Phase Permanent-Magnet Synchronous Motor Drive System With Luenberger Observers for Motor Line Current Reconstruction," *IEEE Transactions on Industry Applications*, vol. 50, no. 4, pp. 2602–2613, 2014. DOI: 10.1109/TIA.2013.2296625.

[89] T. Mitsui and Y. Iwaji, "Motor current reconstruction method using single shunt resistance by high-frequency voltage injection," in *2022 International Power Electronics Conference (IPEC-Himeji 2022- ECCE Asia)*, 2022, pp. 2280–2285. DOI: 10.23919/IPEC-Himeji2022-ECCE53331.2022.9807215.

[90] A. Hino and K. Wada, "Resonance Analysis Focusing on Stray Inductance and Capacitance of Laminated Bus Bars," *IEEJ Journal of Industry Applications*, vol. 5, no. 6, pp. 407–412, DOI: 10.1541/ieejjia.5.407.

[91] T. Asada, Y. Baba, N. Nagaoka, A. Ametani, J. Mahseredjian, and K. Yamamoto, "A Study on Basic Characteristics of the Proximity Effect on Conductors," *IEEE Transactions on Power Delivery*, pp. 1790–1799, 2017. DOI: 10.1109/TPWRD.2016.2590962.

[92] P. L. Dowell, "Effects of Eddy Currents in Transformer Windings," in *The Institution of Electrical Engineers*, vol. 113, 1966, pp. 1387–1394.

[93] J. Jacobus D. van Wyk, W. A. Cronje, J. D. van Wyk, C. K. Campbell, and P. J. Wolmarans, "Power Electronic Interconnets: Skin- and Proximity Effect-Based Frequency Selective Multipath Propagation," *IEEE Transactions on Power Electronics*, pp. 600–610, 2005. DOI: 10.1109/TPEL.2005.846549.

[94] A. Djordjevic, R. Biljie, V. Likar-Smiljanic, and T. Sarkar, "Wideband frequency-domain characterization of FR-4 and time-domain causality," *IEEE Transactions on Electromagnetic Compatibility*, vol. 43, no. 4, pp. 662–667, 2001. DOI: 10.1109/15.974647.

[95] B. Liu, W. Li, D. Meng, *et al.*, "Low-Stray Inductance Optimized Design for Power Circuit of SiC-MOSFET-Based Inverter," *IEEE Access*, vol. 8, pp. 20 749–20 758, 2020. DOI: 10.1109/ACCESS.2020.2964687.

[96] D. Han and B. Sarlioglu, "Comprehensive Study of the Performance of SiC MOSFET-Based Automotive DC-DC Converter Under the Influence of Parasitic Inductance," *IEEE Transactions on Industry Applications*, vol. 52, no. 6, pp. 5100–5111, 2016. DOI: 10.1109/TIA.2016.2586463.

[97] K. Mitsui and K. Wada, "Design of a Laminated Bus Bar Optimizing the Surge Voltage, Damped Oscillation, and Switching Loss," *IEEE Transactions on Industry Applications*, vol. 57, no. 3, pp. 2737–2745, 2021. DOI: 10.1109/TIA.2021.306129.

[98] B. Lu, V. Pickert, J. Hu, *et al.*, "Determination of Stray Inductance of Low-Inductive Laminated Planar Multiport Busbars Using Vector Synthesis Method," *IEEE Transactions on Industry Electronics*, vol. 67, no. 2, pp. 1337–1347, 2019. DOI: 10.1109/TIE.2019.2899547.

[99] K. Mitsui and K. Wada, "Analysis of Clearance Effect for Perforated Terminals Isolation of a Laminated Busbar to Parasitic Parameters," in *The 2022 International Power Electroncis Conference (IPEC-Himej 2022 -ECCE Asia-)*, Himeji, Hyogo, 2022, pp. 1171–1178. DOI: 10.23919/IPEC-Himeji2022-ECCE53331.2022.9806999.

[100] H. Lutzen, K. Mitsui, K. Wada, and N. Kaminski, "Optimistion and Proof of Concept Studies for the M-Shunt Structure applied to Printed Circuit Boards," in *CIPS 2020; 11th International Conference on Integrated Power Electronics Systems*, Berlin, Germany, 2019.

[101] C. Svensson and G. Dermer, "Time domain modeling of lossy interconnects," *IEEE Transactions on Advanced Packaging*, vol. 24, no. 2, pp. 191–196, 2001. DOI: 10.1109/6040.928754.

[102] A. Z. Khalf, "Ferroelectric Glass-Ceramic Systems for Energy Storage Applications," in *Advanced Ceramic Materials*, M. Mhadhbi, Ed., Rijeka: IntechOpen,

2020, ch. 2. DOI: 10.5772/intechopen.93855. [Online]. Available: https://doi.org/10.5772/intechopen.93855.

[103] T. Hong, O. Lesaint, P. Gonon, and H. Debruyne, "Effect of humidity on the high voltage characteristics of epoxy/glass insulation," in *Proceedings of the 2004 IEEE International Conference on Solid Dielectrics, 2004. ICSD 2004.*, vol. 2, 2004, 628–631 Vol.2. DOI: 10.1109/ICSD.2004.1350509.

[104] S. Hashino and S. Toshihisa, "Separation measurement of parasitic impedance on a power electronics circuit board using TDR," in *2010 IEEE Energy Conversion Congress and Exposition*, 2010, pp. 2700–2705. DOI: 10.1109/ECCE.2010.5618046.

[105] A. J. Marques Cardoso, "Power electronics design methods and automation in the digital era: Evolution of design automation tools," *IEEE Power Electronics Magazine*, vol. 7, no. 2, pp. 36–40, 2020. DOI: 10.1109/MPEL.2020.2988077.